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RECORD CELL EFFICIENCIES ON mc-Si AND A ROADMAP TOWARDS 20%, THE EC PROJECT TOPSICLE

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ABSTRACT: Record cell efficiencies were achieved with newly developed processes. An integral approach from wafer to module was used. Starting with high-purity feedstock, high-quality large-area mc-Si wafers were made and characterized. Initial lifetimes of up to 160 µs were observed. Three cell concepts were developed further to obtain high efficiency cells: 1) based on screen-printing and complete inline processing; 2) based on V-grooved texturing and roller printing; 3) based on a hybrid buried contact concept with screen-printed Al BSF. With advanced inline processing an independently confirmed efficiency of 17.0% was achieved on 156 cm^2 mc-Si, which is a record for complete inline processing. A full size module made of cells processed with this process has a peak power of 94.3Wp, which corresponds to an encapsulated cell efficiency of 16.8%. Roller printing on V-grooved cells resulted in an independently confirmed efficiency of 17.2%. With the hybrid buried contact concept an efficiency, again independently confirmed, of 18.1% was reached on a cell area of 137 cm^2; a record for this size. This record cell was used to determine a roadmap towards 20% mc-Si cell efficiency. For that, it is mainly needed to improve the rear side passivation and rear side internal reflection. This can be done with a di-electric layer for passivation and local contacts. Furthermore, the shading losses should be reduced with for example the Angled Buried Contact concept.
Keywords: Multi-Crystalline, High-Efficiency, Manufacturing and Processing

1 INTRODUCTION

One of the requirements to make 1 €/Wp multi crystalline silicon (mc-Si) PV technology available is to increase today's solar cell efficiencies significantly. This can only be achieved if high-quality mc-Si wafers become available, and if an appropriate high efficiency and industrially feasible processing sequence can be developed. The European project TOPSICLE [1] has dealt with this research from feedstock to module. ScanWafer made high-quality mc-Si wafer material. All other partners were involved in detailed characterization of this new high-quality material and in cell process development. UKON, NaREC and BP Solar focussed their research on the buried contact concept. ECN Solar Energy and SCHOTT Solar concentrated their research on the screen-printed process sequence. UKON and UPM-IES were involved in the development of novel processes.

This paper will show the characteristics of the high-quality material and the highest cell efficiency achieved using different process schemes. Furthermore, possible ways to obtain 20% mc-Si PV technology will be presented.

The focus of the research was to obtain the highest efficiencies. Although the developed processes were tested on batches smaller than about 50 wafers, a first estimate on costs and environmental impact was made as well.

2 EXPERIMENTAL

2.1 Material optimization and characterization

Several batches of high-quality 12.5×12.5 cm^2 wafers with a thickness of 325 µm were made using high-purity feedstock material and the best available crystallization procedure. The material was characterized using selected wafers from across the full ingot and carrying out:

- Lifetime measurements with the Quasi Steady-State Photo conductance technique [2] after passivating both surfaces with either SiN_x:H or iodine-ethanol;
- Substitutional carbon concentration [C_s] with Fourier Transform Infra Red (FTIR) spectroscopy;
- Interstitial oxygen concentration [O_i] with FTIR;
- Interstitial iron concentration [Fe_i] from lifetime measurements before and after illumination (dissociation of the FeB pairs);
- Baseline cell processing based on screen-printing and firing-through SiN_x:H.

The effect of gettering during phosphorus diffusion and hydrogen passivation from SiN_x:H layers on the lifetime and [Fe_i] was investigated as well.

2.2 Cell processing and modules

Three high-efficiency process schemes were developed during the project:

- A completely inline process with isotexturing, screen-printed metallization and firing-through SiN_x:H;
- A mechanical V-textured, roller-printed metallization and firing-through SiN_x:H;
- Hybrid buried front contact with screen-printed Al Back Surface Field (BSF) and V-grooved texturing.

The process flows are presented in Table I in more detail. For all process schemes large area mc-Si were used.

Current-Voltage (IV) characteristics of the cells were performed according to the ASTM-E948 norm [3]. The best cells were sent to Fraunhofer ISE CalLab for independent measurements. The Internal Quantum Efficiency (IQE) was determined from the spectral response and reflection.

Table I: Process sequences

Completely in-line based on screen-printing	V-grooved texture and roller printing	Hybrid buried contact
Advanced isotexturing	Mechanical V-texturing	Mechanical V-texturing
Belt furnace emitter process (>70 Ω/sq)	$POCl_3$ emitter (~50 Ω/sq)	Light emitter diffusion (~100 Ω/sq)
Microwave PECVD SiN_x:H	PECVD SiN_x:H	LPCVD SiN_x
Screen-printed front and rear metallization	Front side roller and rear side screen printed metallization	Grooving front side and cleaning
Simultaneous firing	Simultaneous firing	Deep groove diffusion
		Print Al and BSF formation
		Metallization

2.3 Possible improvements and roadmap towards 20%

The best cells were evaluated in detail using PC-1D 5.5 [4]. Using this simulation tool individual parameters were fitted in such a way that both the IV and IQE correspond to the measured values. Based on this evaluation and a loss analysis using a program similar to IQE1D [5] (called "SR" and written by Fischer [6]) possible improvements were quantified, and used to make a roadmap towards 20% cell efficiency.

3 RESULTS AND DISCUSSION

3.1 Material optimization and characterization

Three different batches of "TOPSICLE material" were made and characterized in detail. Fig. 1 shows an example of lifetimes dependent on the position in the ingot. From 2 columns the initial lifetime is presented and for 1 column the lifetime after gettering is depicted as well. From the figure it can be seen that very high initial lifetimes above 150 µs are found. Gettering was carried out on wafers from column B, and it was observed that the lifetime increased by about 50 µs. Fig. 2 shows the corresponding $[Fe_i]$ of the columns presented in Fig. 1. It can be seen that $[Fe_i]$ is reduced to $2\text{-}3\times10^{10}$ cm^{-3} after gettering. At these low concentrations $[Fe_i]$ will not affect the cell efficiency. Passivation from SiN_x:H resulted in an additional improvement of the lifetime. Dependent on the initial material properties, an improvement of 20 to 50 µs was observed.

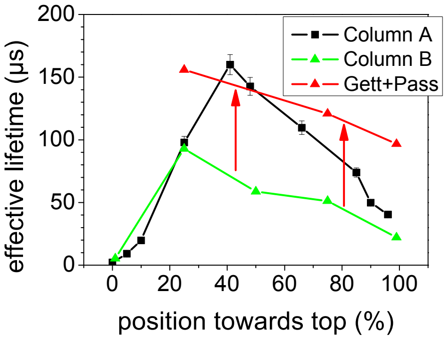

Figure 1: Initial lifetime of columns A and B as a function of the position in the column. The improved lifetime of column B after gettering is presented as well.

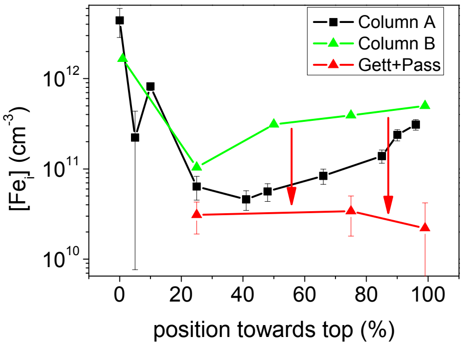

Figure 2: Initial $[Fe_i]$ over column A and B. The lower $[Fe_i]$ after gettering for column B is presented as well.

Fig. 3 shows typical plots of $[C_s]$ and $[O_i]$ as a function of the position in the column. Since both concentrations are below 10 ppm it is expected that there is no influence on cell output. Maybe for $[C_s]$ between 5 and 10 ppm there will be a minor effect.

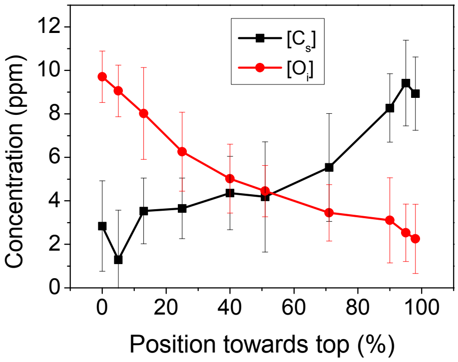

Figure 3: Typical $[C_s]$ and $[O_i]$ over a column of TOPSICLE material.

Baseline processing was applied to make solar cells with the TOPSICLE material. With the better columns efficiencies of around 16% have been obtained, which means that the better TOPSICLE material is as good as the better commercially available material.

3.2 Cell processing and modules

Completely in-line processing based on screen-printing

Advanced inline isotexturing using an acidic mixture based on HF/HNO$_3$ was used for improved light confinement. Applying this process results in very low reflectivity. At a wavelength of 1000 nm and in the absence of an anti-reflection coating, the reflection of is around 10% (see Fig. 4), which is comparable to the reflection of a pyramid texture on mono material. The gain in cell output for this advanced process is 3% relative with respect to industrial isotexturing. The latter has a gain of about 5% relative compared to alkaline etching. The in-line diffusion was carried out with a standard belt furnace. The sheet resistivity was about 70 Ω/sq. The process was optimized in such a way that no lifetime degradation was observed on float zone Si material. Microwave PECVD SiN$_x$:H was applied as antireflection coating and for bulk and surface passivation. An H-pattern Ag front side and full Al rear side for Back Surface Field (BSF) formation were screen-printed and both contacts were fired simultaneously. This optimized process resulted in an independently confirmed efficiency of 17.0% [7]. The IV parameters are shown below:

V_{oc}=624 mV, J_{sc}=35.4 mA/cm^2, FF=0.770, η=17.0%
Cell size: 156 cm^2.

This process was applied to a batch of about 50 wafers. The efficiency distribution is depicted in Fig. 5. The average efficiency of these 50 cells is 16.8%. A first full-size module was made from this batch using cover glass with an antireflective layer. The output of this module (Fig. 6) is 94.3Wp, which corresponds to an encapsulated cell efficiency of 16.8% (not independently confirmed).

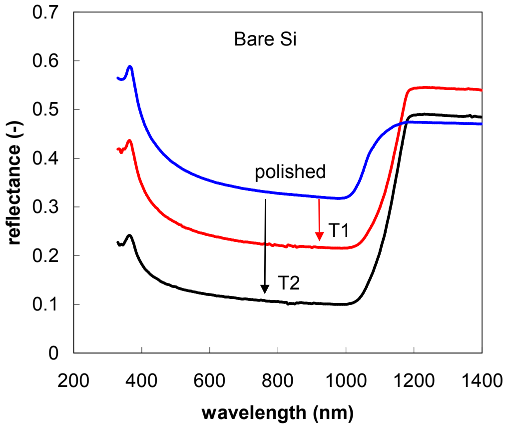

Figure 4: Reflection curves of bare silicon: polished, industrial isotexturing T1, and advanced isotexturing T2 resulting in an additional gain of 3%.

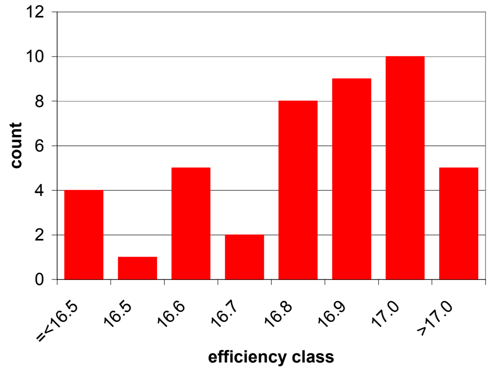

Figure 5: Efficiency distribution of about 50 cells processed with a completely inline process sequence.

Figure 6: Full size module with screen-printed cells and an encapsulated cell efficiency of 16.8%.

V-grooved texture and roller printing

Screen-printed solar cells normally have a shading loss of about 8%. Using V-grooved texturing and roller printing, this loss can be reduced to about 5.5% [8]. The principle and a cross section of a roller printed line are presented in Fig. 7. It can be seen that the optical width of such a line is only 30 µm. This reduced shading and improved V-grooving was applied to a solar cell and resulted in an independently confirmed efficiency of 17.2%. The IV parameters are:

V_{oc}=624 mV, J_{sc}=35.9 mA/cm^2, FF=0.767, η=17.2%
Cell size: 151 cm^2.

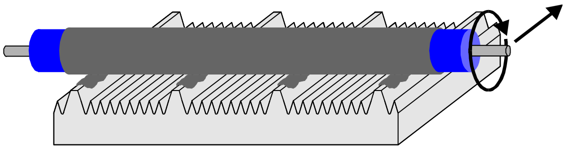

Figure 7a: Principle of roller printing

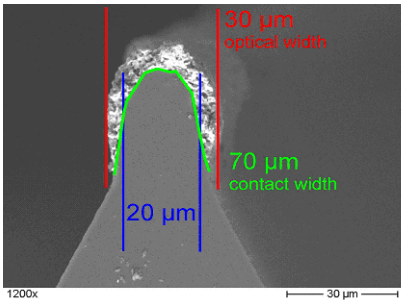

Figure 7b: Cross section of roller printed metallization finger.

Hybrid buried contact design

Polix mc-Si wafers were used to obtain the highest efficiency with the hybrid buried contact process. The concept is shown in Fig. 8 and the process is as shown in Table I. Further improvement of the process that resulted in 17.6% efficiency [9] has resulted in a record efficiency of 18.1% [10]. This efficiency is independently confirmed by ISE CalLab. The cell characteristics are:

V_{oc}=636 mV, J_{sc}=36.9 mA/cm^2, FF=0.770, η=18.1%
Cell size: 137.7 cm^2.

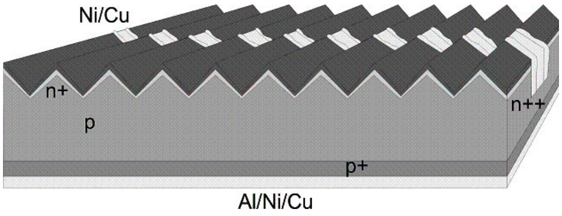

Figure 8: Cross section of the buried contact cell with V-grooved texture.

3.3 Possible improvements and roadmap towards 20%

The 17.0% screen-printed cell [7] and the 18.1% hybrid cell [10] were analyzed in more detail to determine possible improvements. A loss analysis of the 18.1% cell is used to define a roadmap towards 20% cell efficiency.

Possible improvements for screen-printed cell

The IQE of the 17.0% was calculated from its spectral response and reflection. The IQE of a Float Zone cell made with the same process was used as a reference. The characteristics of that cell are:

V_{oc}=624 mV, J_{sc}=35.6 mA/cm^2, FF=0.778, η=17.3%
Cell size: 148 cm^2.

For modeling, the bulk lifetime for the FZ cell was assumed to be 1000 µs, which means that the cell efficiency is not limited by the material lifetime. Then S_{rear} and R_{rear} were fitted with PC-1D in such a way that the IQE at longer wavelengths correspond to the measured ones. These S_{rear} and R_{rear} were used to fit τ_{bulk} of the 17.0% mc-Si cell. S_{front} was fitted to the IQE at shorter wavelengths. After that, final adjustments of the resistances were made to obtain the same IV results as were modeled with PC-1D. The results can be seen in Fig. 9 and Table II. There is excellent agreement between the modeled parameters and experimental values (see also 3.2).

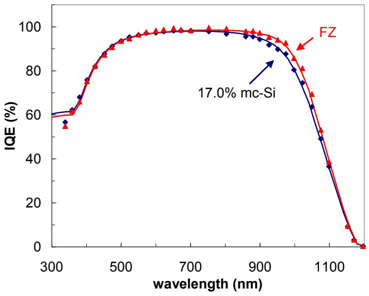

Figure 9: Measured and fitted IQE (using PC-1D) of the 17.0% mc-Si solar cell and its FZ reference.

Table II: Results of fitting the 17.0% screen-printed mc-Si cell using PC-1D.

Property / cell parameter	FZ reference	17.0% mc-Si (screen printing)
τ_{bulk} (µs)	1000	90
S_{front} (cm/s)	2.7×10^5	2.5×10^5
S_{rear} (cm/s)	350	350
R_{rear} (%)	67	67
modeled V_{oc} (mV)	624	624
modeled J_{sc} (mA/cm^2)	35.9	35.4
modeled FF	0.777	0.771
modeled η (%)	17.4	17.0

From Table II it can be concluded that the efficiency is limited by both the front and rear side. The applied front side consists of a homogeneous emitter with a sheet resistivity of about 70 Ω/sq. Up to now we were not able to contact emitters with sheet resistivities of about 100 Ω/sq and low dopant concentrations at the surface (<10^{20} cm^{-3}). A selective emitter process could reduce the losses and result in a high-efficiency emitter without additional resistance losses. The rear side is limiting as well. Applying di-electric passivating layers combined with good quality local BSF and contacting will result in even lower recombination velocities and internal reflectivities above 90%. Furthermore, the shading losses of the front side metallization should be reduced. With standard screen-printing the shading losses are around 8%. Advanced screen-printing on lab scale could reduce this, for example using multiprinting with which lines with an aspect ratio of about 1 are obtained (see Fig. 10) [11]. Roller printing on V-grooved textured material is another option. However, all this does not seem to be enough to obtain 20% efficiency. A buried contact design is a more promising way to go.

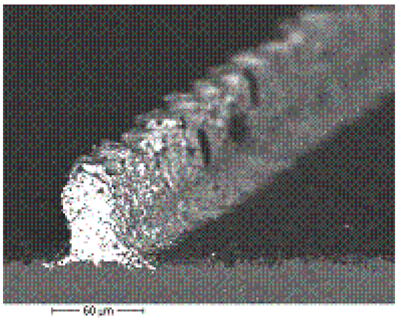

Figure 10: High aspect ratio finger obtained with multiple printing. The width and height are both about 60 µm.

Hybrid buried contact design

Buried contact cells have a selective emitter. In the grooves there is a highly doped layer resulting in low contact resistance. Between the fingers there is a lightly doped emitter. Furthermore, the shading losses are much less than those of screen-printed cells. Fig. 10 shows the IQE of the 18.1% cell compared to the previously obtained 17.6% cell [9]. The IQE at longer wavelengths is better due to higher τ_{bulk}, lower S_{rear} and better R_{rear}. Clearly visible is the better IQE of the buried contact cells at shorter wavelengths with respect to the screen-printed cell, which explains the much higher V_{oc} for the hybrid buried contact cell.

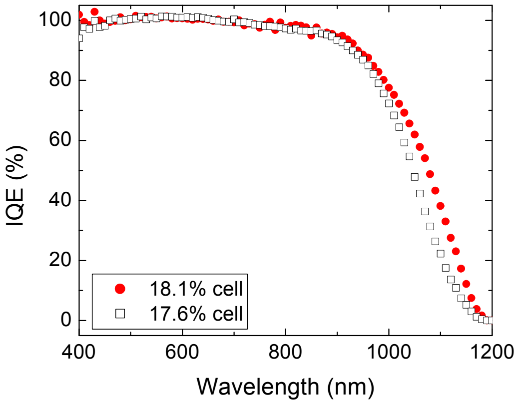

Figure 10: IQE of the 18.1% hybrid buried contact cell and that of the previously made 17.6% cell.

Roadmap towards 20%

The 18.1% cell is used to determine a roadmap towards 20% cell efficiency. Detailed results can be found in [10]. PC-1D was used for modeling. Improvements to obtain this ultra-high efficiency should be in *FF*, R_{front}, S_{rear} and R_{rear}, τ_{bulk}, S_{front}, and lower shading losses by using an Angled Buried Contact (ABC) design [12]. The plating process of the 18.1% cell could be further optimized resulting in *FF*=0.79, which is not unrealistic, and will result in an efficiency gain of 0.4% absolute. R_{front} can be improved by adjusting the layer thickness of the SiN_x layer. This will result in 0.1% absolute higher efficiencies. Instead of an Al BSF a dielectric layer combined with local contacts/BSFs can be applied resulting in S_{rear} of about 200 cm/s and R_{rear} of 95%. This will result in 0.6% absolute higher efficiency. There is still some room for improved bulk material. A lifetime of above 55 µs will give another 0.1% absolute. There is also room for improvement in front surface passivation. A stack of oxide and nitride could improve S_{front} from 14000 to 8000 cm/s, which will increase the efficiency by 0.2% absolute.

The final efficiency improvement should be realized by another cell design, the ABC concept in which the grooves are made at an angle (see Fig. 11). This will eliminate the shading loses completely and result in an efficiency gain of 0.6% absolute. First results with the ABC concept have given efficiencies close to 15% and are encouraging [12].

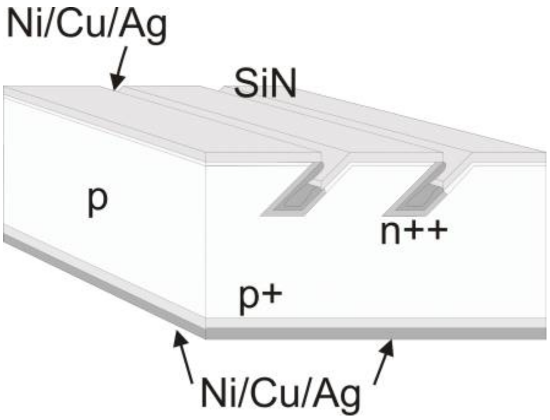

Figure 11: Cross section of the ABC (Angled Buried Contact) cell design.

With all the improvements described above the total efficiency gain will be 2% absolute with respect to 18.1%, and results in just over 20% cell efficiency. The final modeled cell parameters are:

V_{oc}=643 mV, J_{sc}=39.6 mA/cm^2, *FF*=0.79, η=20.1%

3.4 Assessment

Although the main focus of the project was to achieve high efficiencies, and not industrialization, a first cost and environmental assessment was made. The costs relative to an industrial process with an efficiency of 15.5% are presented in Fig. 12. This first estimate shows that the ABC concept should result in about 2% higher efficiencies to be cost effective with respect to the screen-printed one. This higher efficiency should come from the absence of shading losses and possibilities to improve the front surface passivation.

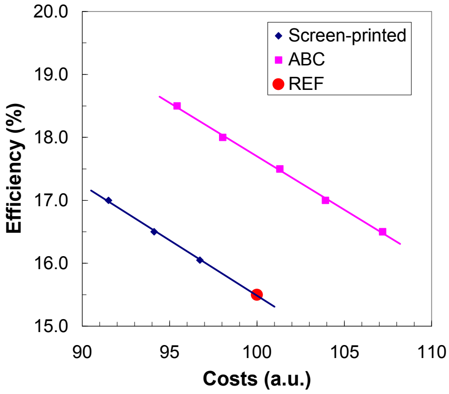

Figure 12: Costs per Wp for screen-printed and ABC process with respect to 15.5% industrial process.

Just as reducing costs was not a main focus, the same holds for environmental aspects. A comprehensive study on the developed processes was carried out with respect to national legislation and the EC directives [13]. For all newly developed processes, a limited environmental effect is expected. All emissions will be below 10% of the limits when the exhaust of chemical and furnace processes is purified or recycled. All this can be done with state-of-the-art technologies.

4 CONCLUSIONS

Starting with high-purity feedstock, high-quality large-area mc-Si wafers were made. Initial lifetimes up to 160 µs were observed. Gettering improved the material quality by about 50 µs resulting in lifetimes above 100 µs over almost the whole column. Three cell concepts were developed further to obtain high cell efficiencies. With advanced inline processing an independently confirmed efficiency of 17.0% was achieved on 156 cm^2 mc-Si, which can be seen as a record for completely inline processing. A batch of about 50 mc-Si wafers was then processed with this 17% process to make a full size module. The peak power of that module is 94.3Wp, which corresponds to an encapsulated cell efficiency of 16.8%.

Roller printing on V-grooved cells resulted in an independently confirmed efficiency of 17.2%.

With the hybrid buried contact concept an efficiency, also independently confirmed, of 18.1% was reached with 137 cm^2 mc-Si, a record for this size. This record cell was used to define a roadmap towards 20% mc-Si cell efficiency. For that, it is mainly needed to improve the rear side passivation and rear side internal reflection. This can be done with a di-electric layer for passivation and local contacts. Furthermore, the shading losses should be reduced, or better eliminated, with for example the Angled Buried Contact concept.

First costs calculations show that the developed processes can result in lower costs per W_p.In the case of the Angled Buried Contact design the efficiency should be about 2% absolute higher than that of the screen-printed concept to be cost effective. An environmental analysis showed that all emissions will be below 10% of the limits when the exhaust of the processes is purified or recycled.

5 ACKNOWLEDGEMENTS

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6 REFERENCES

[1] EC's FP5 programme: ENK6-CT2002-00666

[2] R.A. Sinton and A. Cuevas, Appl. Phys. Lett. **69** (1996) 2510.

[3] www.astm.com

[4] P.A. Basore, D.A. Clugston, PC-1D v5.5, University New South Wales 2000.

[5] R. Brendel and R. Plieninger (1996) *IQE1D, Program for the analysis of solar cell quantum efficiency measurements*, Vertrieb Garching Innovation GmbH Munich.

[6] B. Fischer (2003) *Loss Analysis of Crystalline Silicon Solar Cells using Phtotoconductance and Quantum Efficiency Measurements*, Cuvillier Verlag, Göttingen ISBN: 3-89873-804-3.

[7] C.J.J. Tool *et al.*, Proceedings 20th EPVSEC Barcelona 2005., 578

[8] F. Huster *et al.*, Proceedings 17th EPVSEC Munich, 1743.

[9] W. Jooss *et al*. Proceedings WCPEC-3 Osaka 2003.

[10] M. McCann *et al.*, Proceedings WCPEC-4 Hawaii 2006.

[11] B. Raabe *et al.*, Proceedings 20th EPVSEC Barcelona 2005, 930

[12] M. McCann *et al*, Proceedings 20th EPVSEC Barcelona 2005, 737

[13] B. Lenkeit *et al.*, this conference, 2DV.2.52