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17% mc-Si SOLAR CELL EFFICIENCY USING FULL IN-LINE PROCESSING WITH IMPROVED TEXTURING AND SCREEN-PRINTED CONTACTS ON HIGH-OHMIC EMITTERS

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ABSTRACT: A simple in-line industrial process has been developed for commercial multicrystalline silicon (mc-Si) which results in solar cells with an average efficiency of 16.5%. The best cell has an independently confirmed efficiency of 17.0%. These are the highest efficiencies reported for full inline processing. The process consists of an acidic etch for texturing, homogeneous spin-on phosphorous and a belt furnace emitter diffusion, MicroWave PECVD of silicon nitride layers, and screen-printed metallization. The silicon nitride layer serves as antireflection coating and provides bulk and surface passivation. Detailed characterization and computer simulation show that implementation of already proven technologies in the current cell processing can lead to efficiencies around 18%.
Key words: multicrystalline Si, passivation, texturization

1. INTRODUCTION

The trend towards cost-effective multicrystalline silicon (mc-Si) PV technology is to use large and thin wafers and obtain high efficiencies. It is expected that 210×210 mm^2 wafers with a thickness of 200 µm will be applied in the near future. It will be difficult to handle these fragile wafers in today's high-efficiency processes where the wafers are placed vertically in batch systems, such as for $POCl_3$ diffusion and parallel-plate plasma-enhanced chemical vapor deposition (PECVD) for passivating layers.

It has been postulated that high efficiencies could only be obtained when clean batch processes such as $POCl_3$ diffusion are used and that selective emitters would be required. The purpose of this work is to demonstrate a simple in-line industrial process that results in mc-Si solar cells with efficiencies of over 17.0%. The described process is an improved process compared to the process with which we obtained 16.8% [1].

A belt-furnace diffusion for a homogeneous emitter combined with acidic texturing and in-line MicroWave Remote PECVD and screen printing is used to obtain the 17% mc-Si solar cell technology. With this process an important step towards the development of an industrial process for high efficiencies (>18%) on large (>400 cm^2) and thin (~150 µm) wafers is made. Advanced cell concepts needed for these large and high-efficiency cells will be discussed at the end of the paper.

2. EXPERIMENTAL

A simple industrial process sequence was used for solar cell processing. It consists of the following process steps: acidic etching for combined saw damage removal and texturing, belt furnace emitter diffusion with the wafers directly on the metal belt, MicroWave Remote PECVD of silicon nitride (SiN_x:H), screen-printed metallization and firing (see Table 1). 156 cm^2 mc-Si wafers from different commercial suppliers (wafers A, B and C) with thickness of around 300 µm were used for solar cell processing. Float zone Si was used as a reference to quantify the losses at the rear side of the cell (recombination losses and reflection) in more detail. Two different texturing recipes were tested on two mc-Si wafer types. No post-treatments like applying a second layer anti-reflection coating, forming gas anneal (FGA) or additional edge isolation were carried out.

To check the effect of possible contamination from the metal belt during diffusion *p*-type FZ Si was used. The lifetime was measured on an unprocessed FZ wafer and on an FZ after diffusion. The emitter was removed from the diffused wafer and both surfaces of the FZ wafers were coated with a surface passivating SiN_x:H layer (see Table 2). The effective lifetime was measured using the Quasi Steady-State Photo Conductance technique [2].

Current-voltage (IV) measurements were performed using the class A solar simulator at ECN with six current probes per busbar. The measurements were performed according to the ASTM-E948 norm [3]. The best cell was measured at Fraunhofer ISE Callab in Freiburg, Germany, for confirmation. The Internal Quantum Efficiency (IQE) was determined from spectral response measurements and reflectance measurements.

To determine series resistance losses contact resistance mapping was performed with the Corescan. [4].

PC-1D5.5 [5] was used for modelling to identify which improvements are necessary to increase the efficiency to 18%.

Table 1: Simple in-line solar cell processing on 156 cm^2 mc-Si wafers and 148 cm^2 FZ wafers.

Advanced in-line solar cell processing sequence
1. Recipe T1 and T2 acidic etching for saw damage removal and surface texturing (T1 is being used in the industry)
2. 65-80 Ω/sq emitter (depending on material and texture) made by spin-on phosphorous source and infrared heated belt furnace emitter diffusion
3. Edge isolation
4. SiN_x:H deposition with MicroWave Remote PECVD system, single layer with refractive index n=2.1-2.2
5. Screen-printing of the Ag front side and full Al rear side metallization
6. Simultaneous firing of the front and rear side metallization and Al Back Surface Field (BSF) formation using an infrared heated belt furnace..

Table 2: Process scheme for lifetime checking of the diffusion.

Step	Reference	Diffusion
1	-	emitter formation
2	-	emitter removal
3	lifetime measurement	lifetime measurement

3. RESULTS AND DISCUSSION

3.1 Cell results

Two different acidic etching recipes were used. Recipe T1 is currently being used in the industry. It results in a reflectance of about 20% at 1000 nm on bare silicon and a 6% gain in J_{sc} compared to alkaline etched mc-Si cells [5]. Recipe T2 is a newly developed recipe which results in a 10 to 12 % lower reflectance over the whole wavelength range (Figure 1), and in an additional 3% increase in J_{sc} compared to texture T1 [1]. This means that recipe T2 results in a gain in Jsc of 9% with respect to alkaline-etched cells. Figure 2 shows the difference in surface structure between etch T1 and etch T2. Etch T2 results in a much finer texture. Figure 3 shows the reflectance curves after applying a SiN_x:H anti-reflection coating (ARC).

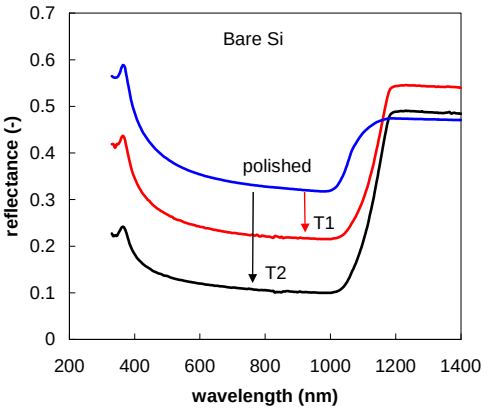

Figure 1: Reflectance of bare silicon wafer after texturization.

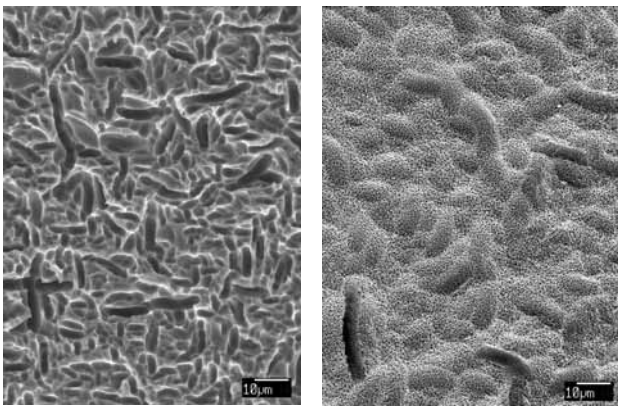

Figure 2: SEM micrograph of industrial texture T1 (left) and newly developed texture T2 (right).

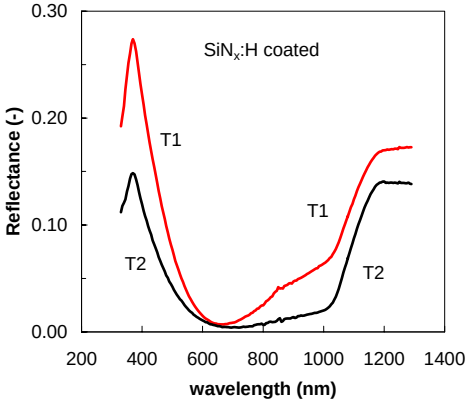

Figure 3: Reflectance of cells with either the industrial texturing process T1 or the newly developed texturing process T2. Cells are coated with a SiN_x:H ARC.

The effective lifetimes τ_{eff} of a *p*-type FZ wafer before diffusion and of an FZ wafer after diffusion were the same (360 µs) and limited by the surface passivation. This means that the lifetime does not degrade during our belt diffusion. For the cell processing emitters with sheet resistivities between 65 and 80 Ω/sq were used. To obtain good contacting on these lightly doped emitters the homogeneity is important. We have optimised our diffusion process for 80 Ω/sq emitters resulting in a standard deviation in sheet resistivity of <3 Ω/sq. This homogeneous and high sheet-resistivity emitter could be contacted successfully. This is illustrated in Figure 4 with a Corescan of a cell with our improved emitter resulting in FF=77%. This scan also shows the good homogeneity of both our emitter process and our fring.

The IV results of the different groups are presented in Table 3. The best efficiencies for the different groups are presented in the upper half of the table. The best cell was sent to Fraunhofer ISE Callab for calibration and shows an efficiency of 17.0% (see Figure 5).

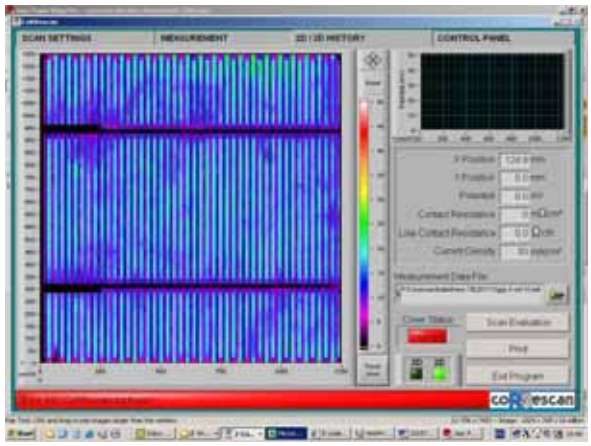

Figure 4: Corescan contact resistance map of a cell with improved high resistivity emitter. The average contact resistance is 5-10 mΩcm^2.

The average values of the IV characteristics for all wafer types and both textures are presented in the lower half of Table 3. The group size was 10-15 cells, expect for group A/B, T2/70. This group consist of 40 cells from wafer types A (different ingots) and B, is textured with T2, and has a 70 Ω/sq emitter. The efficiency distribution of this group is presented in Figure 6, and it can be seen that 19 cells have efficiencies above 16.5%. The 3% difference in J_{sc} between both textures can be seen from the average J_{sc} values of the wafer B groups (T1/80 and T2/80).

Table 3: IV characteristics averaged over the group and of the best cell for both materials used. The data for the 17.0% cell are measured by Fraunhofer ISE Callab. Texture type and emitter sheet resistivity are included.

wafer	Texture /emitter	J_{sc} mA/cm^2	V_{oc} mV	FF %	η %
A: best cell	*T2/70*	*35.4*	*624*	*77.0*	***17.0***
A: best cell	T1/80	35.0	626	76.9	16.8
B: best cell	T2/80	35.2	621	76.3	16.7
C: best cell	T1/65	34.5	622	77.7	16.7
FZ	T2/70	35.6	624	77.8	17.3
A/B: average	T2/70	34.9	617	76.5	16.5
A: average	T1/70	34.7	626	76.1	16.5
B: average	T1/80	33.6	610	75.7	15.5
B: average	T2/80	34.7	614	76.4	16.3
C: average	T1/65	34.4	621	77.0	16.4

Our best values for V_{oc} and J_{sc} have been obtained on wafer type A when textured with T2 and with an 80 Ω/sq emitter. The best V_{oc} observed is 631 mV and the best J_{sc} is 35.5 mA/cm^2. Unfortunately we were not able to contact this wafer type, texture and emitter combination. Good contacting should result in an efficiency of about 17.2% [1].

To investigate the limitations of our processing FZ material was used as a reference. The same processing as applied to mc-Si was used for the FZ material: texture T2 and a 70 Ω/sq emitter. The IQE of the 17.0% mc-Si is compared to that of the 17.3% FZ cell in Figure 7, and it can be seen that the only difference is at the longer wavelength, which is due to the better bulk lifetime in FZ material.

3.2 Comparison to previous results

To quantify our progress made since the 19th EPVSEC in Paris 2004, IV results of our record cells are summarized in Table 4, and the IQEs of the cells are shown with respect to the 17.0% cell in Figure 8. The best cell presented at the Paris conference [7] has an emitter of 65 Ω/sq, that of the Orlando 2005 presentation 80 Ω/sq [1], and that of the 17.0% presented here 70 Ω/sq. The texture T2 for the 17.0% is really different from the T1 (see Figure 2). This means that this cell shows a gain in current due to improved light coupling, but some losses due to less effective surface passivation (emitter and texture). This is confirmed by the IQE ratios presented in Figure 8. The blue responses of the 16.5 and 16.8% cells are better than that of the 17.0% cell. However, the bulk and/or rear side of the 17.0% is somewhat better. The better texturing for the 17.0% cell is dominating and results in a better efficiency.

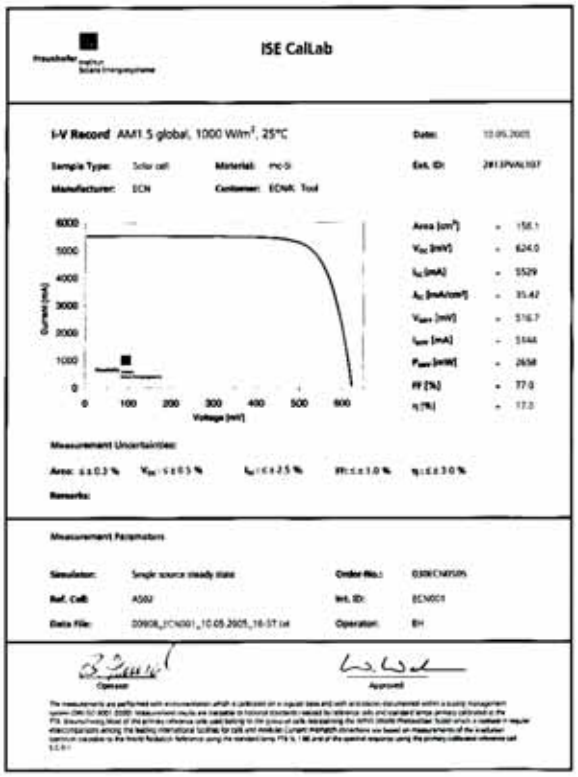

Figure 5: Calibration report of the 17.0% mc-Si solar cell.

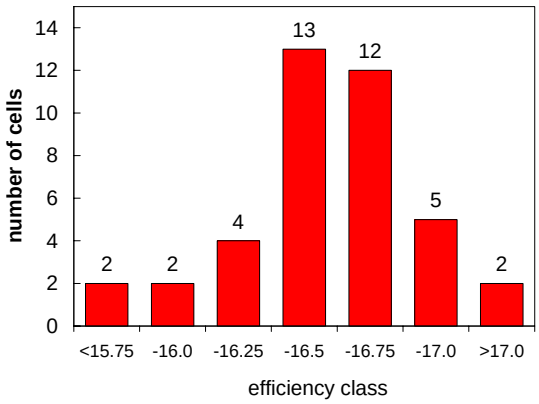

Figure 6: Histogram of efficiencies for wafer type A and B with texture T2 and a 70 Ω/sq emitter.

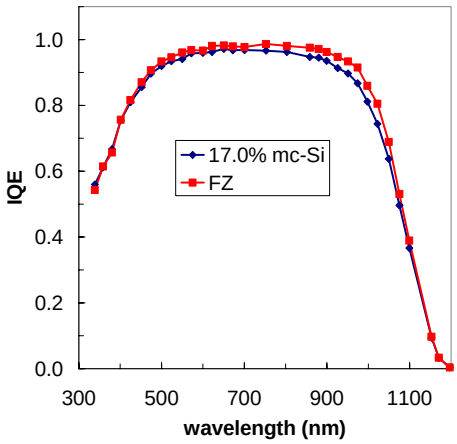

Figure 7: IQE of the 17.0% mc-Si and the 17.3% FZ cell made with the same processing

Table 4: ECN's progress for inline processing. For the future cell improvements discussed in 3.4 are implemented.

Conference	J_{sc} mA/cm^2	V_{oc} mV	FF %	η %
Paris 2004	34.5	623	76.8	16.5
Orlando 2005	35.0	626	76.9	16.8
This one 2005	35.4	624	77.0	17.0
Future	37.0	636	76.9	18.1

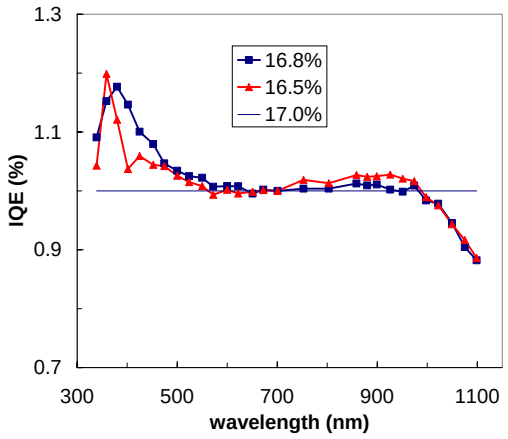

Figure 8: IQE ratios of previously reported cells with respect to the 17.0% mc-Si cell.

3.3 Comparison with worldwide results

Our best V_{oc} and J_{sc} are similar to those of the record large area cell made by Jooss et al. (V_{oc}=632.5 mV, J_{sc}=35.85 mA/cm^2, FF=77.7%, efficiency η=17.6) using a mechanically V-grooved texture, a selective 100 Ω/sq $POCl_3$ emitter and a plated buried contacts [8]. Compared to our 17.0% cell the difference is a 1% relative better V_{oc}, J_{sc} and FF for the record cell. The difference in V_{oc} and J_{sc} can be explained by the higher sheet resistivity of the emitter. The better FF can be explained by the better contact resistance due to the selective emitter used in the Laser Grooved Buried Contact concept.

The 17.7% mc-Si cell of Kyocera [9] has a V_{oc} of 620 mV and a J_{sc} of 37.0 mA/cm^2. For that cell Reactive Ion Etching (RIE) was used for texturing which will result in higher short circuit currents. The IQE for wavelengths longer than 900 nm of our 17.0% cell, which is a measure for the material quality and rear side (passivation and internal reflection), is comparable to that of the 17.7% cell made by Kyocera [9]. Combined with a better V_{oc} of our cell it can be concluded that our processing is comparable to that of Kyocera except for the light coupling.

3.4 Modeling

To determine the limitations in our processing in more detail we have analyzed our results using PC-1D. We have used the procedure as described in our paper presented at the 19th EPVSEC [7]:

- First fit IV and IQE of FZ using τ_{bulk}=1 ms;
- Secondly, use the obtained rear side parameters (S_{rear} and R_{rear}) to fit the mc-Si cell, which means: vary τ_{bulk} of the mc-Si to fit IQE between 800 and 1200 nm;
- Then, final adjustments of S_{front} and J_{O2} to fit IV, and IQE between 300 and 700 nm.

The result can be seen in Figure 9 and Table 4. Furthermore, improved parameters have been used for PC-1D calculations to determine the efficiency potential. Reducing the effective S_{front} to 5×10^4 cm/s will increase the efficiency to just below 17.5%. This better font side will result in an IQE at 400 nm just above 80%, which was observed in our textured 16.8% mc-Si solar cell presented at the 31st IEEE PVSC [1]. The effect of improving rear side (both S_{rear} and R_{rear}) and the τ_{bulk} simultaneously is depicted in Figure 10. High lifetimes up to 150 µs can be obtained on mc-Si wafers after gettering and passivation [10]. The parameters for the improved S_{rear} and R_{rear} have been observed in separate experiments [11,12]. Both the bulk and rear side improvements are needed to obtain 18% efficiency. Moreover, figure 10 shows that the effect of improving the rear side is larger for the better lifetimes. For τ_{bulk}=90 µs the improved rear side will give a 0.3-0.4% absolute efficiency gain, while for τ_{bulk}=150 µs it will be 0.4-0.5% absolute.

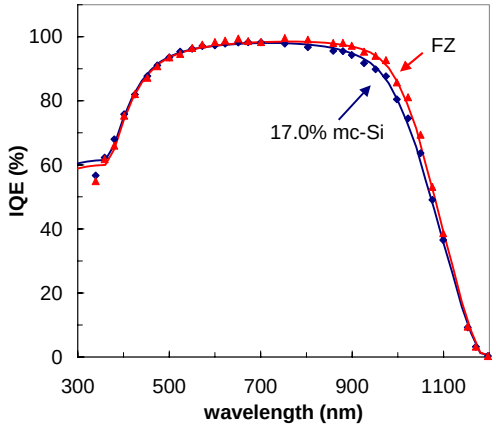

Figure 9: PC-1D fitting of the FZ and 17.0% mc-Si cell.

Table 4: PC-1D fitting of FZ and 17.0% mc-Si cell. Improvements to obtain 18% are also given.

property/ cell output	FZ	17% mc-Si	improved (18%)
τ_{bulk} (µs)	1000	90	150
S_{rear} (cm/s)	350	350	200
R_{rear} (%)	67	67	80
S_{front} (cm/s)	$2.7 \cdot 10^5$	$2.5 \cdot 10^5$	$5 \cdot 10^4$
modeled V_{OC} (V)	0.624	0.624	0.636
modeled J_{SC} (mA/cm^2)	35.9	35.4	37.0
modeled FF	0.777	0.771	0.769
modelled η (%)	17.4	17.0	18.1

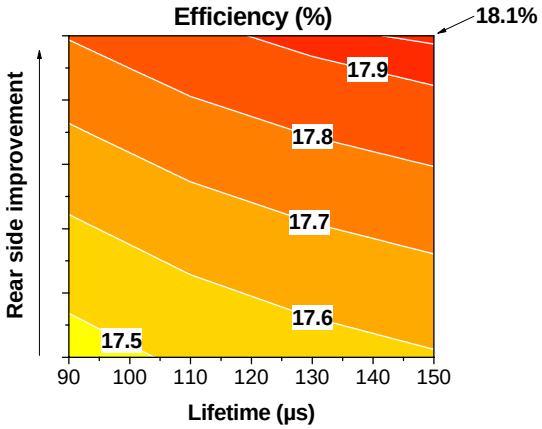

Figure 10: Contour plot of the effect of improving the rear side (S_{rear} from 350 to 200 cm/s and simultaneously R_{rear} from 67 to 80%) and τ_{bulk} (from 90 to 150 µs) on the efficiency. Starting point was our best cell with improved front surface passivation and an efficiency of 17.5%.

4 LONG TERM DEVELOPMENTS

For the long term the presented cell concept and process has some drawbacks for thin (~150 µm) and large (>400 cm^2) cells:

- A full Al rear side will cause too much bowing;
- The surface recombination of an Al BSF will not be good enough to obtain very high efficiencies;
- The internal rear side reflection R_{rear} of about 80% will cause additional losses in J_{sc} for thin wafers;
- An H-pattern metallization will cause extra shading and series resistance losses. For example, using two busbars for a 210×210 mm^2 cell will require more lines per unit length. More busbars will make the cells less attractive.
- Interconnection of large and thin cells is hardly possible with the current tabbing design. J_{sc} of 210×210 mm^2 cells will be 15-16A. This is about a factor 3 higher than the current industrial 156 cm^2 cells. This will require more or thicker tabs, and thus shading losses and possible cell breakage.

The non-ideal passivation and light trapping at the rear will result in an efficiency loss of about 0.5% absolute going to 150 µm thin solar cells. This in combination with the other points make that new cell and module concepts are needed for future mc-Si PV technology at low costs.

A possible new design that does not have the above-mentioned limitations is PUM [13] with advanced rear-side processing. The PUM cell presented in Figure 11 has 16 small holes in which the emitter contact is printed through. With these vias the PUM cells can be interconnected from the rear side. For improved rear side passivation a di-electric layer can be used together with good quality local BSFs and local contacts. An additional layer is needed to ensure perfect light trapping. Advantages of PUM are:

- Easy module manufacturing because the interconnection is carried out at the rear;
- More output and better appearance, the metallization coverage is about half of that of cells with an H-pattern.
- Series resistance losses are independent on the size of the cell, but only depend on the size of the unit cell around the holes.

For this cell concept the bulk lifetime will not limit the efficiency when the diffusion length is about 4 times the thickness of the cell. For a 150 µm thin cell this will be for lifetimes of about 120 µs, which have already been observed for mc-Si material [10]. With ideal surface passivation and perfect light management this should result in cell efficiencies around 20%.

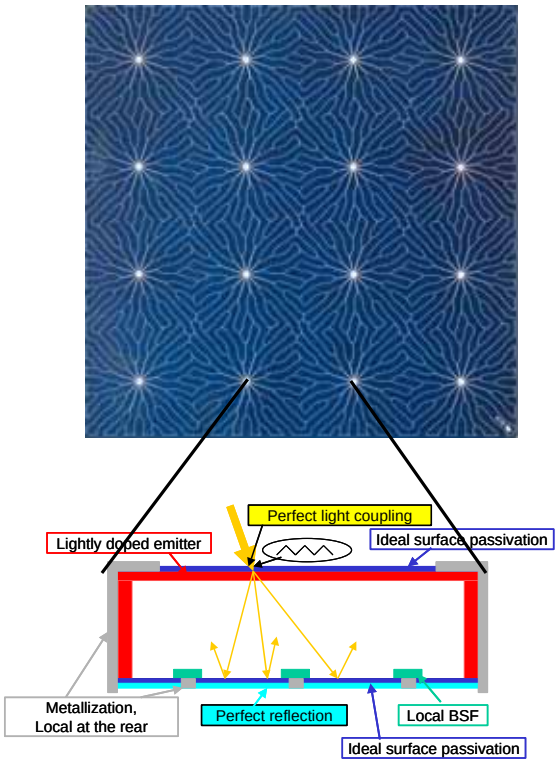

Figure 11: PUM cell and a cross section between the holes. The emitter contact is printed through holes for rear side interconnection.

Even more ideal will be a completely back contacted solar cell such as the cells that are manufactured by

SunPower [14]. This cell design has no metallization on the front, and thus no shading losses. An example of a completely back contacted cell can be seen in Figure 12. For this cell the limiting length is not the thickness, but the collection length, i.e. the distance between location of generation and that of collection. For very thin cell this means that the distance between the local emitters determines the requirements for material quality. That this cell concept can result in 20% efficiencies in production has been demonstrated for thick FZ material [14].

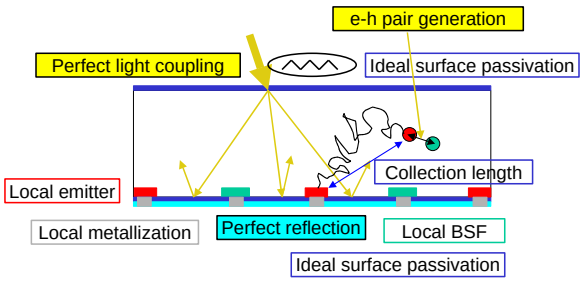

Figure 12: Cross section of a completely back contacted solar cell. Local emitters and local contacting are at the rear side. Ideal passivation between the contacts is needed for high efficiencies.

5 CONCLUSIONS

It is shown that completely in-line cell processing with belt furnaces can be used for high-efficiency solar cell processing. τ_{eff} of FZ material does not degrade during emitter diffusion on a standard metal belt.

With the in-line process a 17.0% confirmed efficient 156 cm^2 mc-Si solar cell was made using wet chemical texturing, a homogeneous emitter and firing through SiN_x:H combined with screen printing. PC-1D modelling showed that 18% cell efficiency could be achieved when improved processes are implemented in the current cell processing.

For large (>400 cm^2) and thin (~150 µm) high-efficiency (>18%) mc-Si solar cells new cell designs are needed, and our developed process can be seen as a first step for this.

ACKNOWLEDGEMENTS

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