

## Ribbon-Growth-on-Substrate: Status, Challenges and Promises of High Speed Silicon Wafer Manufacturing

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### **ABSTRACT**

The Ribbon-Growth-on-Substrate (RGS) silicon wafer manufacturing technology is a very promising high-speed wafer production technique under development at the moment. It has the promise to lead to a manufacturing technology, which allows silicon wafer manufacturing at the 25 MWp/a to 50 MWp/a level.

A future development of this technology in the areas, RGS machine prototyping, wafer quality improvement and solar cell process optimization should lead to a commercialization of this technology in 2005.

In the following an outline of the past developments, a status of the RGS technology today and the most probable road ahead is presented.

### **Motivation**

In the last years a remarkable growth of the PV industry with annual growth rates well above 25% was achieved [1]. It is expected that PV can and will maintain growth rates at 25 to 35% in the foreseeable future [2]. This also means that the PV industry has to adjust its manufacturing capacities to satisfy the market.

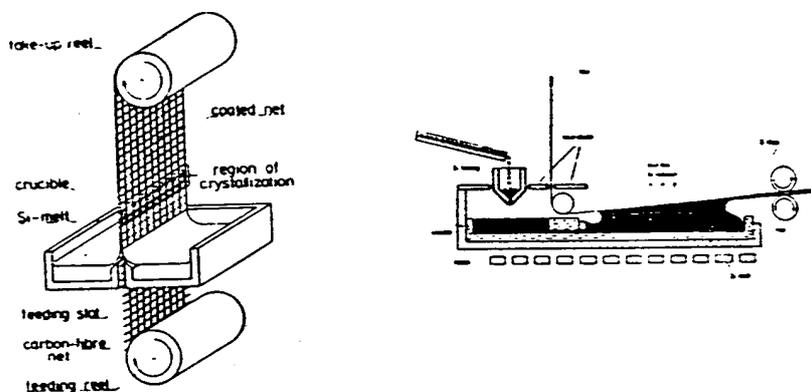
*Table 1: Production speed and capacity of different silicon ribbon production technologies. The last column shows the number of furnaces for a 100 MWp production line. [3] (EFG: edge defined film fed growth, SR: string ribbon)*

Material	Pull speed (cm/min.)	Throughput (cm <sup>2</sup> /min.)	Furnaces per 100 MWp
EFG	1.7	165	100
SR	1 – 2	5 – 16	1175
RGS	600	7500	2 – 3

To fulfill this market demand is the main challenge for PV manufacturing technology in the next years. Although it is expected that the world PV market will approach GWp module shipment levels shortly after 2006, the technology to produce PV modules efficiently on the

100 MWp scale is not available yet. Thus technological developments can be expected in all parts of the PV module production chain, from solar grade silicon, over wafer and solar cell manufacturing to module production. In the field of wafer production, the ribbon-growth-on-substrate silicon wafer technology promises the effective production of silicon wafers at low manufacturing costs, at high production rate (see table 1) and with almost 100% silicon usage.

During the late 70's and 80's a number of potentially high-speed crystal growth technologies were developed in laboratories in the US and in Europe. Their main difference were the way how the crystallization heat was removed from the liquid silicon and how the geometrical definition of the wafer was realised. Although a number of these technologies were very promising and successfully demonstrated on the lab-scale, most of the developments were stopped in the late 80's in a development state, where major investment into a production prototype became necessary.



*Figure 1: Web supported silicon ribbon (S-Web) pulling was under development by Siemens. High throughput and 12% efficiency were demonstrated in the early 90's. The major problem was the single use of the supporting web, which was made of very pure and expensive graphite. Brandl GmbH in Germany now owns this technology. [4]*

Among these processes, there were a number of methods where silicon was solidified in contact with another material (substrate or inlay). Wacker, as an example, at that time developed the so-called RAFT technology, which is similar to the RGS technology in the way that a re-usable substrate material was used to grow the silicon wafer. Other technologies under development were the LASS (low angle silicon sheet) technology or the S-web technology as outlined in figure 1.

None of the above mentioned high-speed silicon ribbon technologies made it into production yet. However driven by the strong market pull and the expectation of a rapidly expanding silicon PV industry, some technological development are started (Sharp's rotational solidification), speeded up (RGS) or revived (S-Web).

## **Ribbon-Growth-on-Substrate wafer manufacturing**

### **Promises**

Compared to all other high-speed wafer manufacturing technologies the Ribbon-Growth-on-Substrate technology was under continuous development since its start in 1984 at Bayer

AG in Germany. But similar to the other technologies there was a strong dedication into the RGS development in the late 80's and early 90's resulting in the building of an RGS laboratory infrastructure and two laboratory scale RGS machines. In the time period between 1994 and 1999 major steps in RGS technology development were realized with respect to wafer quality and solar cell efficiency but it was never decided to invest into the pilot scale RGS machine. Nevertheless this situation resulted in a unique possibility for RGS in the late 90's due to the following:

- It is a very promising high-speed silicon wafer manufacturing technology, which demonstrated continuous improvements throughout its development.
- RGS is well understood from a scientific point-of-view, and a number of advanced solar research laboratories are supporting the further development with their know-how.
- Reasonable solar cell efficiencies are demonstrated and there is sufficient know-how available to justify the development of the pilot machine.

This formed the base for a co-operation between Deutsche Solar (as successor of Bayer Solar) and ECN on one side and a Dutch development consortium with support from S'Energy on the other side for a further development of the technology. [5]

### RGS principle

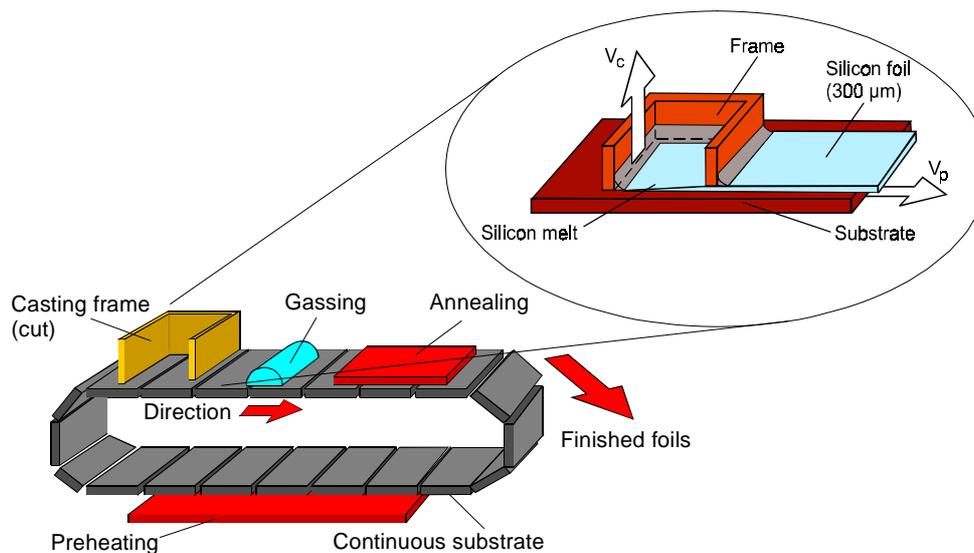


Figure 2: Principle of the RGS process and schematic drawing of the continuous RGS machine built by Bayer. The most important process feature is the de-coupling of the crystal growth velocity ( $V_c$ ) from the production speed ( $V_p$ ) (src. Bayer AG).

The principle of the RGS wafer casting process is simple. A 'cold' (below silicon melting temperature) substrate is moved underneath a casting frame filled with liquid silicon (melting point 1414°C). Thus heat is extracted from the silicon melt forcing a crystallization process of silicon from the substrate into the silicon melt. During this process the substrate is moved underneath the casting frame and crystal growth is stopped at the moment the substrate leaves the casting frame. Thus crystal growth direction and silicon wafer production direction are perpendicular to each other, which allows the independent control of both. Therefore

relatively slow crystal growth can be combined with high substrate transport speed and thus high production volume.

After the casting frame, the wafers and the substrates are cooled down. During this process the wafer and the substrate separate, forced by their different thermal expansion coefficients. This allows the substrate to be re-used after the wafer has been picked-up. The RGS process as shown in figure 2 was demonstrated on Bayer's lab-scale machines.

### Silicon crystal growth process

Silicon crystal growth in contact with a cold substrate can be described by mathematical models, which belong to a class of transient heat transfer problems with a moving boundary condition, the solidification interface. The simplest case of this important class of problems is called the 'classical Stefan problem' [6]. It assumes that a liquid at uniform temperature  $T_l$ , which is higher than the melting temperature  $T_m$  is confined to a half space  $x > 0$ . At time  $t=0$  the boundary surface ( $x=0$ ) is lowered to a temperature  $T_0$  below the melting temperature (i.e. contact with the cold substrate) and maintained at this temperature. As a result solidification starts at the surface  $x=0$  and a solid liquid interface  $s(t)$  moves into positive  $x$ -direction. Under these assumptions the heat conduction equations can be solved and the position of the solid-liquid interface in time is described by:

$$s(t) = \lambda \sqrt{\alpha_s t}$$

with  $\alpha_s$  being the thermal diffusivity of the solid phase and  $\lambda$  being the solution of equation:

$$\frac{\exp(\lambda^2/4)}{\operatorname{erf}(\lambda/2)} + \frac{b}{\sqrt{a}} \frac{T_m - T_l}{T_m - T_0} \frac{\exp(-\lambda^2/4a)}{\operatorname{erfc}(\lambda/2\sqrt{a})} - \frac{\lambda \sqrt{\pi} h_{sf}}{2c_{ps}(T_m - T_0)} = 0$$

with the parameters:

b: ratio of liquid and solid heat conductivity

a: ratio of liquid and solid heat diffusivity

$h_{sf}$ : solidification heat

$c_{ps}$ : specific heat capacity of the solid phase.

Although this model is much too simple to describe the crystal growth in the RGS case, its solution can be useful for the qualitative understanding of crystal growth velocity and wafer thickness.

In dependence of the substrate temperature, the following two figures show the wafer thickness grown after a certain time and the growth velocity of the solid liquid interface.

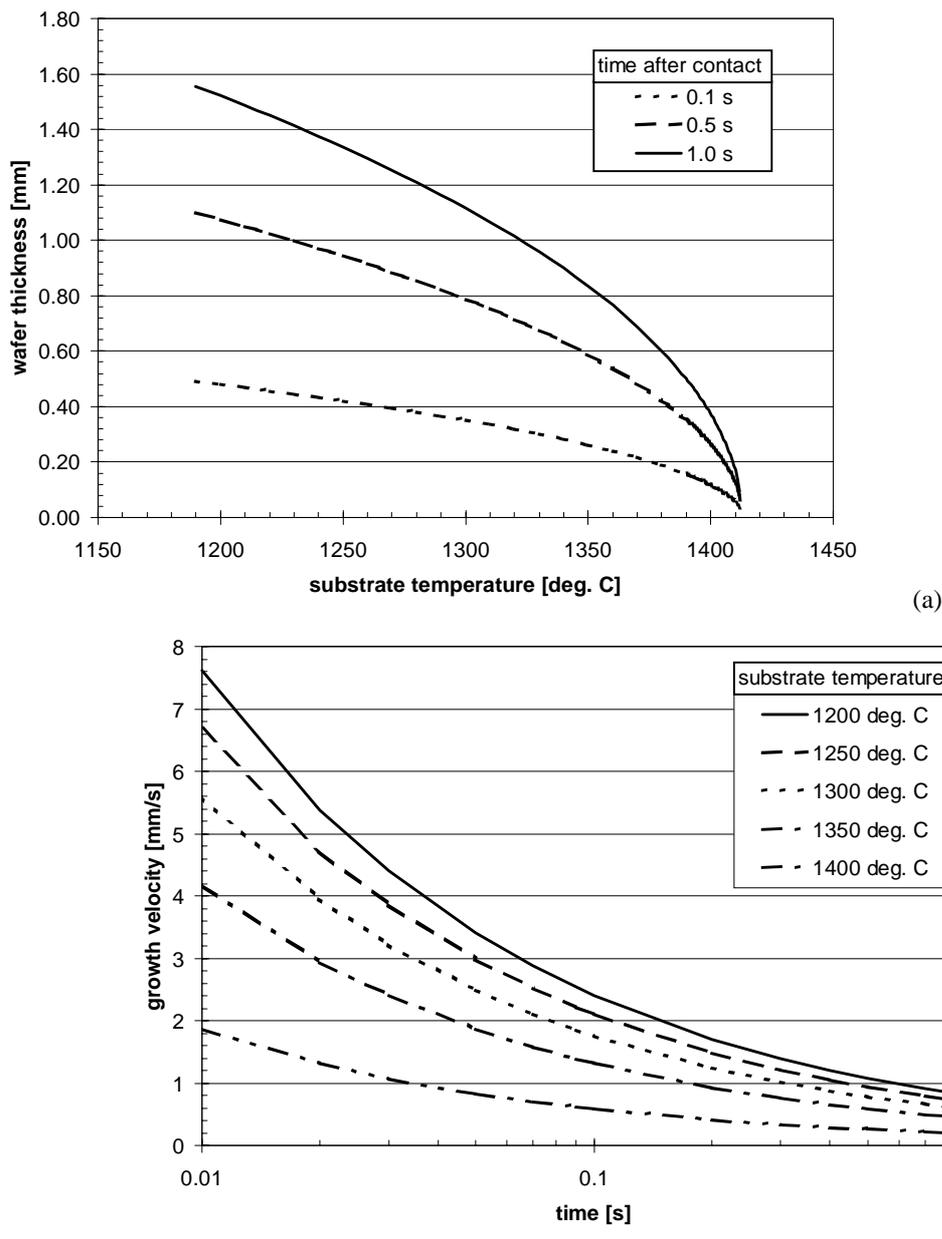


Figure 3: (a) Wafer thickness in dependence of the initial substrate temperature after 0.1s, 0.5s and 1.0s. (b) Growth velocity as a function of time depending on substrate temperature. Note that the analytical expression approaches infinity for  $t \rightarrow 0$ .

As indicated in the figures above, silicon wafer thickness in the range of 0.8 mm up to more than 1.6 mm for reasonable substrate temperatures can be reached in 1 s, with typical growth velocities in excess of a few mm/s range. Compared to other silicon crystallisation methods the silicon crystal growth rate in such a process is very high.

The experimental results from RGS runs are in qualitative agreement with the picture as outlined above, although for a detailed quantitative analysis a much more sophisticated model is needed. In agreement with the classical Stefan problem, the initial crystal growth velocity is high in the beginning of the process and decreases rapidly. However, after a growth period of 1 s, the typical wafer thickness is in the range of 0.3 mm to 0.4 mm, which is much thinner

than predicted by the model. The reason for the overestimation of the wafer thickness by the model is caused by the facts,

- that the substrate temperature is not constant during crystal growth but increasing,
- that there is a finite heat transfer between liquid silicon and substrate, which slows down the crystallisation speed and
- that the liquid silicon melt is most probably in turbulent flow, transporting heat from the hotter top surface of the melt to the liquid-solid interface.

All extensions to the simple Stefan problem solution slow down the crystallisation process, which means, that the solutions above can be regarded as upper limit. In reality, crystallisation speed and wafer thickness is lower, depending on system properties such as silicon-substrate properties, melt temperature and melt behaviour.

### **RGS wafer technology and solar cell process development**

Record solar cell efficiencies achieved with RGS wafer based solar cells show a remarkable trend over the last 10 years. One of the main reasons for this development was the good co-operation between wafer manufacturer (Bayer AG), solar cell process developers as well as basic silicon material research and development (HEXSi, KoSi projects). This led to an increased understanding of the material characteristic and the behavior of the RGS wafer in a solar cell process. The consequences of this development can be seen by the steady efficiency increase as shown in figure 4.

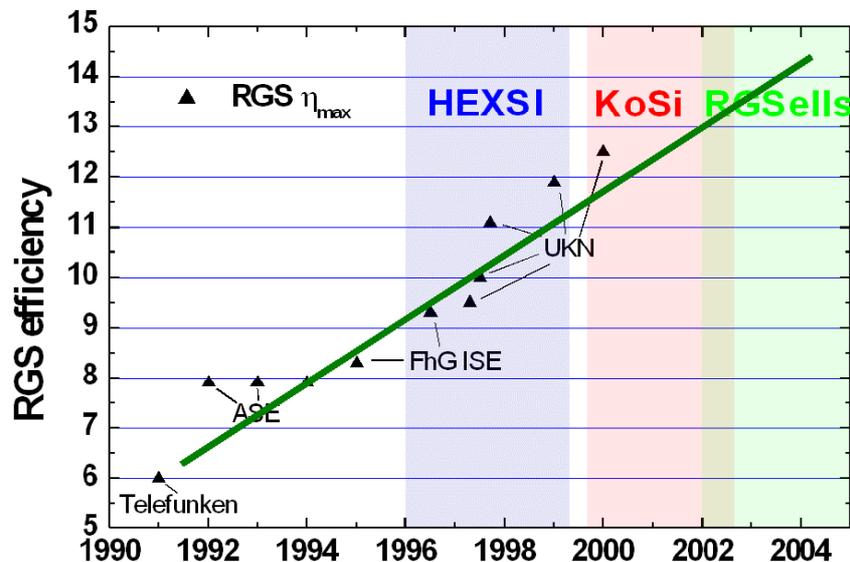


Figure 4: Record RGS solar cell efficiencies. Earliest results were from Telefunken and its successor ASE. In later projects the Fraunhofer Institute for Solar Energy Systems (FhG-ISE) and the University of Konstanz (UKN) held the efficiency records.

In the future, it is expected that this development can be continued at the same or even increased speed. In order to do so, the next improvements in wafer manufacturing will be:

- A reduction of the high oxygen content of the wafers by better silicon melt treatment. The oxygen concentration in the wafer limits at the moment the effect of hydrogen in-diffusion and thus the efficiency of an RGS solar cell in an industrial-type cell process.

The high oxygen content also leads to the formation of oxygen related recombination centers during the cell process (thermal and new donors) [7, 8, 9].

- The application of results from the silicon growth modeling to lower the wafer growth speed further and to improve crystal quality.
- In a second phase the casting process will be optimized to allow better thickness variation control and to lower the amount of liquid silicon film extraction from the casting frame.

Initial steps taken to implement the improvements as outlined above, resulted in the manufacturing of RGS wafers without major shunts, which were regularly seen in the past. These shunts were most probably caused by inversion channels of highly oxygen decorated extended defects, which could in the most extreme cases result in a carrier collecting network in the RGS wafer [10]. In a similar way series resistance problems, which were often lowering the fill factor of RGS wafers, could be solved. Both improvements resulted in the production of the first RGS based solar cell with efficiencies above 10% using an industrial-type solar cell process (i.e. screen printed contacts, firing through silicon nitride ARC, no texturisation).

*Table 2: Cell parameters of an RGS wafer based solar cell produced by an industrial type screen-printing process (cell size 5x5 cm<sup>2</sup>).*

Voc [mV]	Jsc [mA/cm <sup>2</sup> ]	FF [%]	efficiency [%]
563	24.0	75.1	10.1

## **Summary**

Ribbon-Growth-on-Substrate silicon wafer manufacturing technology is one of the most promising technological developments for the further improvement of silicon wafer based PV modules. Its productivity rate in the 25 MWp to 50 MWp range allows the construction of a 100 MWp wafer production facility with only 2-4 RGS machines.

In two R&D projects RGSolar and RGSells, the three important areas of machine development, RGS wafer manufacturing and solar processing are developed in parallel. In the area of machine development, design phase and technical drawing phase is finished resulting in a technical product documentation of the RGS prototype machine. Improvements in wafer manufacturing process development and solar cell processing techniques resulted in better wafer characteristics and a deeper understanding of the factors influencing wafer quality. Main near term challenges are decreasing the oxygen concentration and controlling the crystal growth velocity. Both are accompanied and guided by model forming in the fields of solution and evaporation behavior of impurities in the silicon melt and silicon crystal growth during the casting process.

First steps in reducing the oxygen content resulted in RGS wafers and solar cells, which showed reasonable good cell parameters in a screen-printing process. Promising efficiencies of more than 10% could be achieved. Future improvements in melt treatment should result in further reduction of oxygen concentration and to an increase in solar cell efficiency. Additionally, this new material should react much faster on hydrogen passivation, which makes the material even more compatible with a standard firing through silicon nitride solar cell process.

These results and the promises of high-speed, low-cost silicon wafer manufacturing are the driving force to push this technology forward to commercialization in 2005.

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