

## First xSi cell results using selective emitters formed with diffusion barriers in one step

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### Abstract

A simple and robust selective emitter process is described which uses a selectively screen-printed diffusion barrier layer, deposited before phosphorus diffusion. The method enables an efficiency increase with more than 0.4%, and is suitable for large scale production processes.

### Introduction

The selective emitter process is listed as one of the innovations to be introduced in production of crystalline silicon solar cells. Main requirements are that the efficiency should be increased significantly (more than 0.2%) and the process should be simple and robust [1]. It has been shown that the cell efficiency can be increased by at least 0.2% [2]. Recently, we have introduced a new method for a single diffusion step selective emitter process [3] as an alternative for the method of screen printing selectively a phosphorus dopant paste [2]. Our method uses a selectively deposited diffusion barrier before phosphorus diffusion. Deposition is done by screen printing a paste containing the barrier. After screen printing, the barrier needs to be cured and densified by a drying step at about 500 °C and a barrier layer is formed on the silicon wafer, as is shown in figure 1.

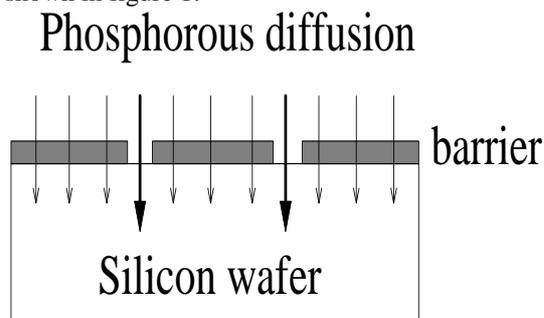


Figure 1. Principle of new selective emitter process.

In case of a belt diffusion, the phosphorus dopant solution can be deposited on this barrier by spraying or spinning. In case of a POCl<sub>3</sub> diffusion, the wafers can be brought into the tube furnace. The diffusion barrier method has many advantages:

1). The adjustment of low level doping is completely independent from the high doping level. The emitter properties beneath the diffusion barrier can be adjusted in three ways. Firstly, the thickness of the layer can be adjusted to change the permeability. Secondly, dopant to the barrier can be added to obtain higher doping beneath the diffusion barrier.

Thirdly, the permeability of the layer can be adjusted by changing the drying conditions to make the layer more or less amorphous.

2). A dead layer is avoided completely because of the very low source of dopants available at the surface.

3). An ideal selective emitter profile can be produced with a step function from low to high doping level.

4). The method can easily be introduced in any production environment because the method of diffusion is not important.

### Results

In figure 2, a SEM picture is shown of the diffusion barrier after sintering with our in-house produced barrier paste. This paste is optimised for printing without slump and curing without cracks. A very homogeneous and 1 µm thick layer has been produced without any cracks, which is an excellent result. Possible cracks might reduce the beneficial effect of the selective emitter, but will not cause shunting of the cell.

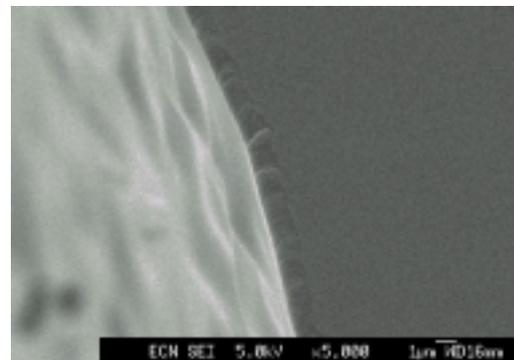


Figure 2: Scanning electron microscope photograph of a SiO<sub>2</sub> barrier layer of 1 µm thickness on top of a silicon wafer viewed in cross section; light material is the surface of the barrier layer.

Using a selectively printed barrier layer, we have produced a selective emitter using standard belt line diffusion by spin-on of a phosphorus source. In figure 3, an emitter sheet resistance line scan across the emitter surface is shown.

This line scan clearly shows that a selective emitter with low and high doping has been produced. In figure 4, a photograph is shown of the wafer after Si<sub>3</sub>N<sub>4</sub> deposition using our remote PECVD system. This photograph shows the colour difference between the highly and lowly doped emitter. When

the emitter is doped more highly, deposition of SiN by remote PECVD is

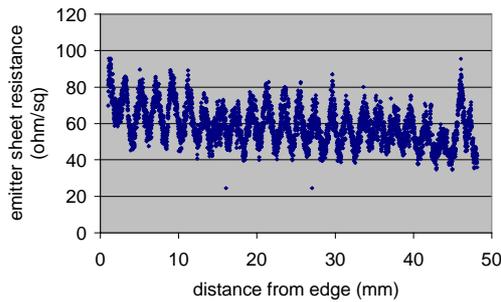


Figure 3: Localised sheet resistance measured from the edge of the wafer.

enhanced due to the larger amount of charge carriers available at the surface. The photograph (fig. 4) shows the homogeneity of the highly doped lighter region and the lowly doped darker region on the wafer.

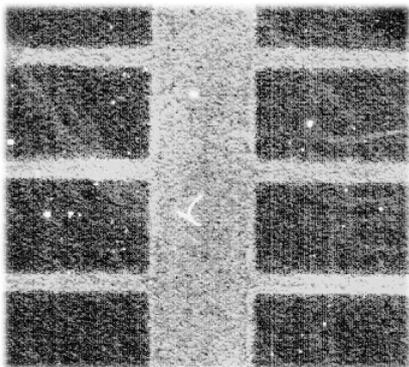


Figure 4 Wafer surface after SiN coating

After the SiN deposition, the cells are finished by screen printing the front and rear contacts and sintering. It is important to align the diffusion barrier and front side metallisation very carefully to avoid shunting. When the alignment is not correct, metallisation will be deposited on a low emitter sheet resistance region. During sintering, the metallisation will etch through the emitter and cause a shunt path. In our laboratory, a semi-automatic Bachini printer is being used. This machine automatically aligns the two print steps within 5  $\mu\text{m}$ , avoiding any chance of shunting. This type of printer is being used in production at speeds of 1000 wafers per hour. Therefore, we conclude that this selective emitter process can be used in production.

In a first test, 25 cells were produced with selective emitter. As a reference, 25 neighbouring cells were made at the same time, without the diffusion barrier formation. In table 1, cell results of the two groups are compared. Both short circuit current and open circuit voltage are about

Table 1: Cell results for 25 reference cells and 25 selective emitter cells

Measured quantity	Reference process	Selective Emitter
Isc [mA/cm <sup>2</sup> ]	29.5	29.8
Voc [mV]	602	607
FF [%]	77.0	76.1
efficiency [%]	13.7	13.8
Shunt [kOhm cm <sup>2</sup> ]	4	4

1% higher for the selective emitter cells. Efficiencies of the two cases are similar due to the lower fill factor of the selective emitter cells that is not caused by the shunt resistance. In figure 5, the internal quantum efficiencies averaged over three cells are compared for the reference and selective emitter cases. The blue response for the selective emitter case is clearly higher as is expected. Lower emitter doping level and lower surface recombination velocities cause this.

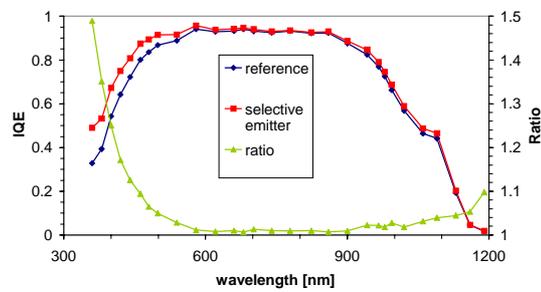


Figure 5 IQE of reference and selective emitter group

## Conclusions

Locally deposited diffusion barriers by screen printing are able to produce a selective emitter. This approach leads to reduced emitter dark saturation currents, causing increased current and voltage, as is shown in this paper. We expect to increase the efficiency using this process by at least 0.4% by adjusting the sheet resistance of the lowly doped region, by improving surface passivation, and by adjusting the design of the front metallisation grid.

## REFERENCES

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