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IDEAL SINGLE DIFFUSION STEP SELECTIVE EMITTERS: A COMPARISON BETWEEN THEORY AND PRACTICE

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ABSTRACT: Selective emitters have been an important research subject for crystalline silicon solar cells for decades. It is being used in production for high efficiency solar cells. In this study, selective diffusion barriers have been used to produce selective emitters. This method allows easy control of the lightly doped areas. Experimentally, selectivity has been confirmed and lightly doped sheet resistances have been varied between 50 and 100 ohm/sq. The produced selective emitter cells showed an increase in current of 2%, an increase in voltage of 1%, and an increase in blue IQE response by a factor of 2. PC1D simulations show that the SiN_x, optimised for mcSi solar cell efficiency, provides some surface passivation. The simulations show that when bulk passivation and short wavelength transmission can be maintained, further gains will be possible with improved surface passivation. For future research, the challenge is to combine the bulk and surface passivating qualities of SiN_x.

Keywords: Silicon - 1: Crystalline - 2: Selective Emitter - 3

1. INTRODUCTION

A selective emitter is an emitter that is heavily doped beneath the contacts and lightly doped in between the contacts. The need for a selective emitter stems from the fact that a high doping level is needed for low contact resistance due to the fact that contact resistance R_c depends on doping level N_d according to [1]:

$$R_c \sim \exp(1/N_d^{1/2})$$

On the other hand, emitter dark current is strongly dependent on the doping level of the emitter. King calculated dark currents for surface doping levels of 10^{18} cm^{-3} and an emitter thickness less than 0.1 µm [2]. This translates in two demands on the emitter:

a) a good ohmic contact with the front-side metallisation, and
b) good collection properties and low emitter dark saturation currents.

For a) a heavily doped low resistance emitter would meet the needs, whereas b) requires a lightly doped, well-passivated emitter. For cost reasons, a homogeneous emitter is commonly used and a lower efficiency is accepted.

The selective emitter process is listed as one of the innovations to be introduced in the production of crystalline silicon solar cells[1,7]. Main requirements for a cost-effective selective emitter are that the efficiency should be increased significantly (more than 0.2%) and that the process should be simple, robust and cheap [2].

Most of the selective emitter processes require expensive extra masking, etching steps, and a double diffusion process making selective emitters not cost-effective [3]. One method that satisfies these requirements is the method of screen-printing a pattern with a phosphorus doping paste. It has been shown that the cell efficiency can be increased by at least 0.2% [4]. This method has not yet been introduced into production. For this process, the doping level of the lightly doped regions depends strongly on the diffusion furnace and gas flows.

Recently, we have introduced a new method for a single diffusion step selective emitter process [5] as an alternative to this method. In this paper, we study the applicability of this selective emitter process for large-scale production of multicrystalline silicon solar cells. Results of experiments with the ECN method will be discussed. These results will be used us input for modelling, which will lead to insights in the surface passivation of these cells. The surface recombination velocities determined in this way will be compared to results obtained by other groups.

2. EXPERIMENTAL RESULTS

2.1 Selective emitters using diffusion barriers

A first step of ECN's method, see figure 1, is a selective deposition of a diffusion barrier prior to phosphorus diffusion. A paste that contains the barrier component SiO_2 is screen-printed. After screen-printing, the barrier has to be cured and densified by a drying step at about 500 °C.

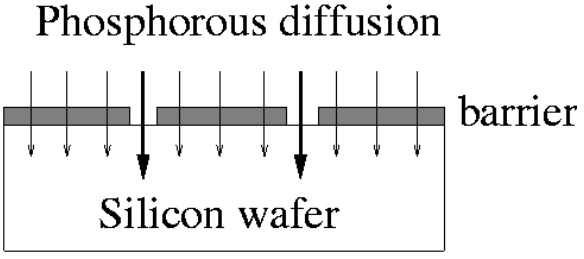

Figure 1 Principle of new selective emitter process.

In case a belt diffusion furnace is used, the phosphorus doping solution can be deposited on this barrier by spraying or spinning. In case a POCl3 diffusion furnace is used, the wafers can be brought into the tube furnace. The diffusion barrier method has major advantages:

1). The adjustment of low level doping is completely independent from the high level doping. The emitter properties beneath the diffusion barrier can be adjusted in

three ways. Firstly, the thickness of the layer can be adjusted to change the permeability. Secondly, doping to the barrier can be added to obtain higher doping beneath the diffusion barrier. Thirdly, the permeability of the layer can be adjusted by changing the drying conditions to make the layer more or less amorphous.

2). A dead layer can be avoided because of the very low source of dopants available at the surface.

3). An ideal selective emitter profile can be produced with a step function from low to high doping level.

4). The method can easily be introduced in any production environment because it can be combined with any diffusion method.

2.2 Deposited diffusion barrier

In figure 2, a SEM picture is shown of the diffusion barrier after sintering with our in-house produced barrier paste. This paste is optimised for printing without slump and curing without cracks. A very homogeneous and 1 µm thick layer has been produced without any cracks, which is an excellent result. Presence of some cracks might reduce the beneficial effect of the selective emitter, but will not cause shunting of the cell.

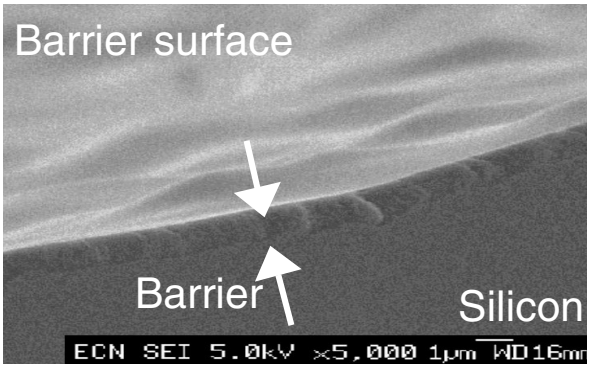

Figure 2: Scanning electron microscope photograph of a sintered SiO_2 layer deposited on a silicon wafer viewed in cross section; light material is the surface of the barrier layer

In figure 3, the active dopant concentration is displayed as a function of depth in the silicon for a sample with and without diffusion barrier, as measured by the Stripping Hall technique. The profile with diffusion barrier clearly has a lower surface concentration and no dead layer.

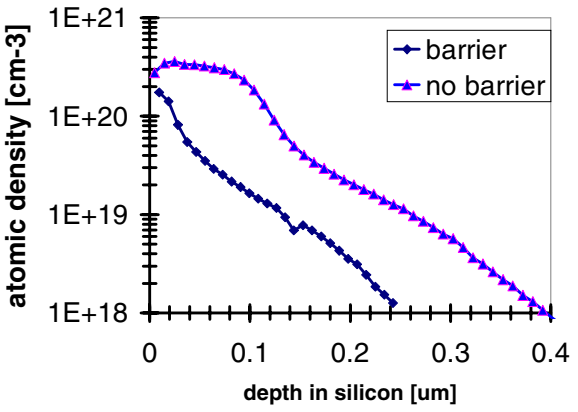

Figure 3: Stripping Hall measured doping profiles for samples with and without diffusion barrier.

2.3 Selectivity of diffusion barrier

Selective emitters have been made on mono Cz silicon wafers according to the following process:

1. Screen-print diffusion barrier paste with varying content of SiO_2 between 0%-20%
2. Sinter barrier layer at 500 °C during 5 minutes
3. Spin phosphorus doping source solution
4. Diffuse at standard settings for a 50 ohm/sq emitter
5. Measure local sheet resistance with a scanning four-point probe measuring device.

In figure 4, the local sheet resistance scans along a line perpendicular to the openings in the barrier layers are displayed. At 10% SiO_2 content, first signs of selectivity can be seen from 50-55 ohm/sq. For 15% SiO_2, selectivity is between 50-75 ohm/sq, and for 20%, selectivity is between 55-85 ohm/sq. The 5% SiO_2 content results in a lower sheet resistance than without a diffusion barrier, which is within variations of the measurement and cell processing. The low sheet resistances of the selective emitters are higher with increasing SiO_2 content. This is due to the measuring probe geometry, which has a distance between the probes of 300 µm, comparable to the width of the opening in barrier layer and thus the low emitter sheet resistance region.

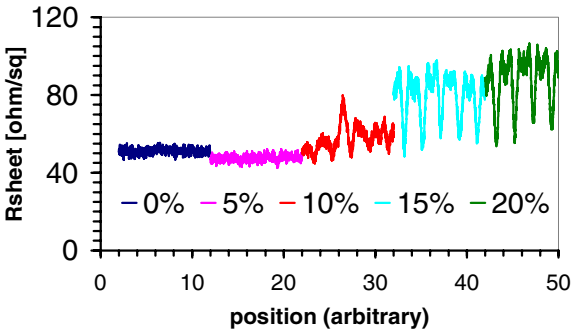

Figure 4 Selectivity of emitter as a function of SiO_2 in barrier paste

3. EXPERIMENT ON MULTICRYSTALLINE SILICON WAFERS

3.1 Experimental set-up

An experiment was set-up using multicrystalline silicon wafers of 100 cm^2 from Baysix material in 5 experimental groups with varying SiO_2 content in the barrier paste, 0%, 5%, 10%, 15%, and 20%. Each group contains 25 wafers, with neighbours of varying material quality distributed between groups to make a reliable comparison from group to group.

All groups were processed according to the processing scheme of table 1, except for the reference group with 0% SiO_2, which did receive neither the screen-print of the barrier paste nor the sintering step. An important aspect of this process sequence is that all steps are carried out in the same way as our standard process. The only additional steps are the printing and sintering of the diffusion barrier paste.

Exact alignment of the barrier paste printing and front side metallisation paste printing is important. This is automatically achieved with the industrial Baccini printer.

The diffusion barrier is completely removed after P-glass removal in a concentrated HF solution. All wafers are hydrophobic afterwards.

Diffusion is carried out in our infrared belt furnace. A comparison between the infrared and resistance heated diffusion process is presented in [6], and a comparison between IR diffusion and POCl3 tube furnace diffusion is presented in an accompanying paper in these proceedings [7].

Finally, the application of a passivating SiN_x is accomplished in the recently introduced Roth&Rau remote PECVD system [8]. This system allows for a large-scale inline production process. The SiN_x process is optimised for the manufacturing of multicrystalline silicon solar cells.

Table 1 Processing scheme for selective barrier process

Selection of neighbouring wafers
Saw damage etch
Screen-print of barrier paste
Sintering @ 500 ^oC
Spin-on of P-source
Diffusion @ 900 ^oC
P-glass removal
SiN_x deposition r-PECVD
Aligned screen-print of front side Ag paste
Drying
Screen-print of rear side Al paste
Firing

3.2 IV results of selective emitters

After processing, all 125 cells were characterised by IV measurement with our class A solar simulator. Also, for a selection of cells, flash J_{sc}-V_{oc} curves were measured according to the method of Sinton [9]. This measurement can be used to calculate the fill factor in open circuit at zero current, which means that no series resistance losses are included in this value. The difference between the series-resistanceless fill factor and the standard fill factor indicates the loss in fill factor due to series resistance losses.

In figures 5-8, the resulting parameters for the 5 groups are compared. Figure 5 indicates a positive correlation between J_{sc} and SiO_2 content, where the difference between 0% and 20% SiO_2 content leads to a 2% increase in current density. Also, V_{oc} and SiO_2 appear to be linearly correlated, leading to a 1% increase in V_{oc} between 0% and 20% SiO_2 content.

However, the fill factors of all cells with a diffusion barrier treatment are significantly lower. For the best case, with 20% SiO_2 content, the reduction in fill factor is 2%, which leads to a marginally higher average efficiency of 14.3% compared to 14.2% for the reference group.

The flash J_{sc} - V_{oc} measurements give an important indication of the cause of these reduced fill factors. According to figure 7, the resistance-less fill factors are all lower by between 0.4% (20% SiO_2) and 1.1% (15% SiO_2). Also, the difference in resistance-less FF and standard FF is higher for cells with diffusion barrier than for the reference cells, as is displayed in table 2.

Series resistance is increased due to the fact that in between the metal fingers, the sheet resistance of the emitter is increased. Using a simple calculation [10], the power loss due to series resistance in the emitter between the fingers is 0.9% for a 50 ohm/sq emitter (reference case) and 1.7% for a 100 ohm/sq emitter (20% SiO_2 content). This is a much lower difference than the 2% as determined experimentally (2.2% against 4.2%).

One way to investigate the cause of this extra series-resistance is with the CoreScan method [11]. In figure 9, a CoreScan is displayed for a cell at 15% SiO_2 content. This shows that a very high contact resistance occurs on one fourth of the wafer. This can be solved by improved process control.

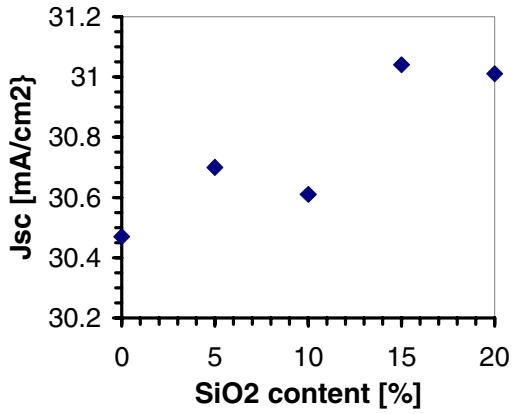

Figure 5: Short circuit current density as a function of SiO_2 content in barrier paste

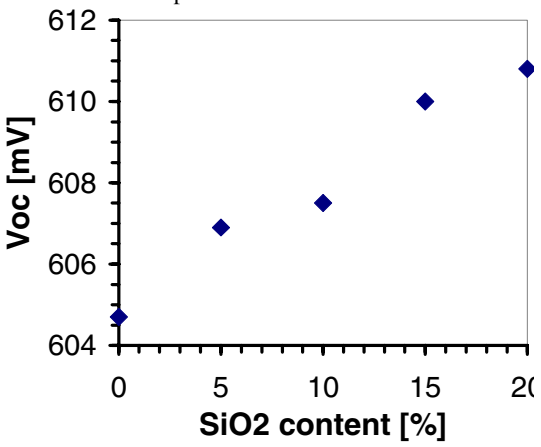

Figure 6: Open circuit voltage as a function of SiO_2 content in barrier paste

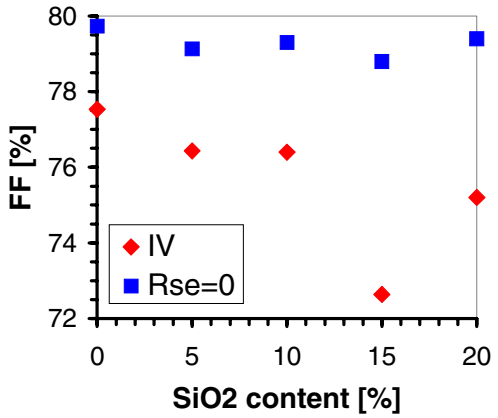

Figure 7 Fill factors as determined by IV measurement and by Sinton measurement (series-resistanceless) as a function of SiO_2 content in barrier paste

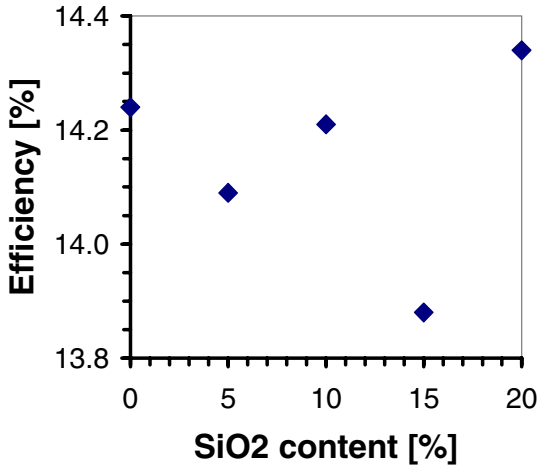

Figure 8: Efficiency as a function of SiO_2 content in barrier paste

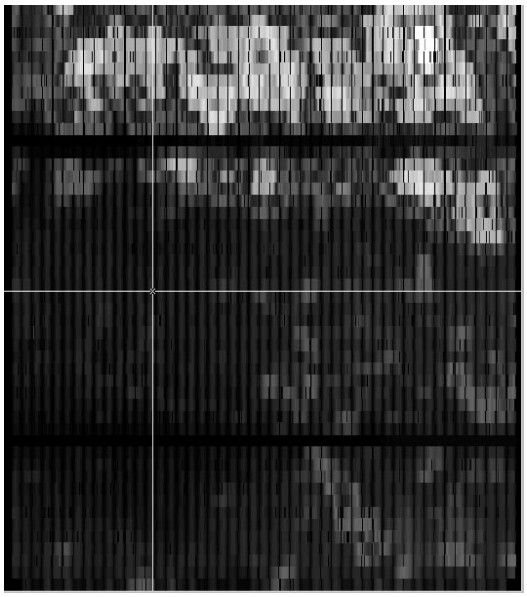

Figure 9: CoreScan of contact resistances measured locally on a cell with reduced fill factor (15% SiO_2 content), light spots indicate higher contact resistance

Table 2: Fill factor reduction due to series resistance

SiO_2 content	0%	5%	10%	15%	20%
Delta-FF	2.2%	2.7%	2.9%	6.2%	4.2%

3.3 Internal quantum efficiencies

In figure 9 and 10, the internal quantum efficiency averaged over three wafers is plotted. The red response (above 700 nm) is the same for all groups.

Furthermore, we can see a clear relation between blue response (<600 nm) and SiO_2 content in the diffusion barrier. The more effective the diffusion barrier is the higher the blue response. Values of 80% IQE below 400 nm, belong to the highest measured at ECN for industrial type processing.

A better blue response is consistent with the theory that more lightly doped emitters lead to lower emitter dark saturation currents and are more easily passivated.

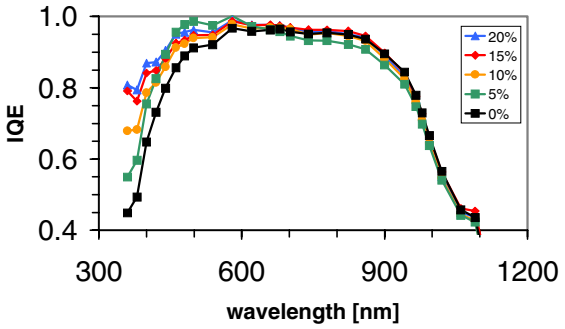

Figure 9: Internal quantum efficiency as a function of wavelength determined for 0% to 20% SiO_2 in barrier paste

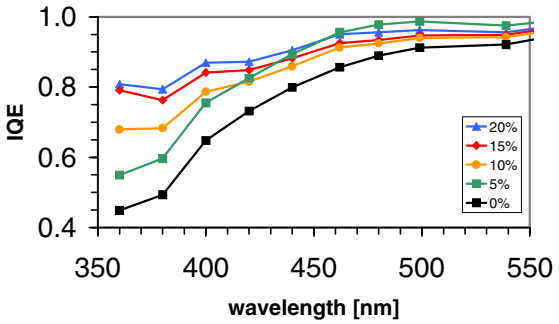

Figure 10: Detail of internal quantum efficiency as a function of wavelength determined for 0% to 20% SiO_2 in barrier paste

3.4 Conclusions and remaining questions

The following conclusions can be drawn from this experiment:

1. Selective emitters produced with diffusion barriers lead to 1% higher V_{oc}, 2% higher J_{sc}, 2% lower FF, and 1% higher efficiency.
2. This increase in V_{oc} is less than we expected from theory and other experiments [3].
3. Fill factor is reduced due to increased diode currents (approximately 0.5%) and increased series resistance in the emitter (approximately 0.8%) and other causes (0.7%).
4. Blue response is improved.

4. MODELLING OF CELL RESULTS

4.1 Goals of modelling

By modelling we want to investigate why the presented results do not show higher efficiency gains for selective emitters. Also, we would like to know what gains would be achievable.

4.2 PC1D model study

We have used the PC1D simulation program to study the cell results [12]. As input, Stripping Hall measured doping profiles have been used. Then, we have adjusted the surface recombination velocity as input to the PC1D model to fit measured internal quantum efficiencies. In this way, we could determine this value accurately. The surface recombination velocity is the quantity to evaluate the surface passivating qualities of a passivating layer on the

emitter. Also, the emitter itself also influences the resulting efficiency.

To show these effects, we have calculated and plotted the influence of surface recombination velocity S on efficiency for two emitter profiles in figure 11. The first emitter profile is for the selective emitter group with 20% SiO_2 content, and the second profile, called industrial, is from our reference group without diffusion barrier. Also, two points are shown, where the internal quantum efficiency corresponds to the experimental data. Several aspects of this graph are of interest:

1. the surface recombination velocities are 10^6 and 10^5 cm/s for the reference emitter and selective emitter (20% SiO_2 content).
2. the calculated efficiency gain for the selective emitter is the same as the experimentally determined gain of 3%, using the calculated surface recombination velocities.
3. this graph shows a strong relation between S and efficiency for both emitters, especially for recombination velocities between 50,000 and 10^6 cm/s. This means that both emitters are transparent for the charge carriers and are sensitive to passivating the surface. Of course, the efficiency of cells with selective emitter depends more strongly on S and that emitter is more transparent.
4. the efficiency does not improve for S values below 10^4 cm/s. For these S values, the efficiency gain using a selective emitter is only 0.2%.
5. the SiN_x provides some surface passivation for the homogeneous, industrial type emitter leading to an efficiency gain of 0.3% compared to a non-passivated emitter.

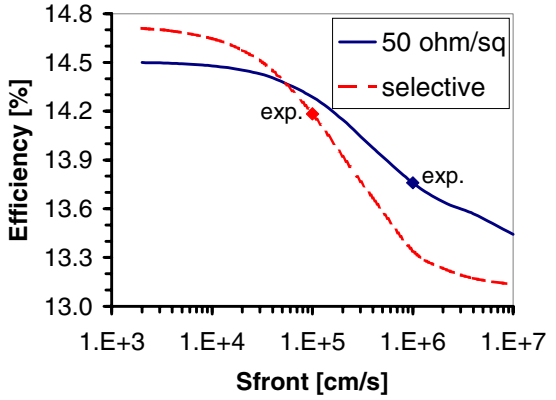

Figure 11: Calculated efficiency as a function of surface recombination velocity, for a homogeneous emitter profile (50 ohm/sq), and a selective emitter profile (20% SiO_2 content), two points are indicated corresponding to S values fitted to experimental IQE values.

4.3 Calculated surface recombination velocities, compared with literature

Using PC1D, we have calculated the surface recombination velocities for the presented experiments. To be able to make a fair comparison, it is important that the emitters that have been passivated are similar, especially regarding the transparency of the emitter for charge carriers. To evaluate the calculated values, we compare these to data recently published by Kerr [13]. These values have been obtained from emitter dark saturation current measurements. S values for SiN_x passivated emitters have been extracted by PC1D simulation.

In figure 12, the surface recombination velocities have been plotted as a function of measured emitter sheet resistance and in figure 13, the surface recombination velocities have been plotted as a function of measured surface dopant concentration. Plotted are values obtained from a fit to the experiment, the published values obtained by Kerr, and values obtained by ECN in the same way as Kerr, for SiN_x optimised for surface passivation [13]. The differences between the plots indicate that surface doping level is not the same for the same sheet resistance.

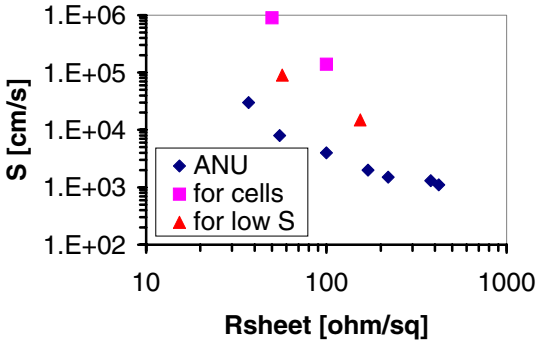

Figure 12: Surface recombination velocity as a function of emitter sheet resistance, for values determined in this study (for cells), ECN values determined for SiN_x (for low S, as it is optimised for surface passivation), and values from literature (ANU, Australian National University) also optimised for surface passivation [13]

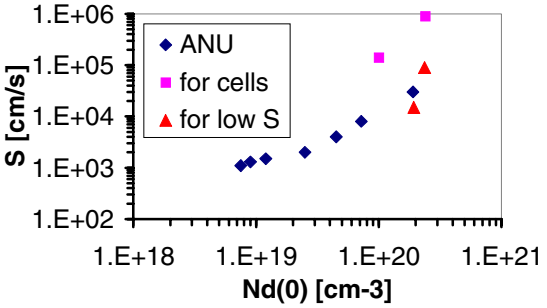

Figure 13: Surface recombination velocity as a function of emitter sheet resistance, for values determined in this study (for cells), ECN values determined for SiN_x (for low S, as it is optimised for surface passivation), and values from literature (ANU, Australian National University) also optimised for surface passivation [13]

These graphs show that SiN_x, optimised for cell processing, lead to much higher S values than SiN_x optimised for surface passivation (either at ECN or ANU).

Bulk passivation of multicrystalline wafers due to the SiN_x is most important in optimising the SiN_x for industrial cell processing. It is unclear why such an optimised SiN_x does not lead to similar surface passivation. Also, surface passivation during contact firing is known to degrade significantly, depending on temperature and time [14].

On the other hand, SiN_x optimised for surface passivation is not suitable for cell processing, because absorption is high for short wavelengths and bulk passivation is poor. Recently, a stoichiometric SiN_x is discovered that exhibit surface passivation and low absorption coefficient at short wavelengths [15]. No

information is available yet whether this SiN_x leads to bulk passivation.

For multicrystalline silicon cell processing, the challenge is to combine the bulk and surface passivating qualities of the SiN_x. When successful, the efficiency gain is 0.7% for a homogeneous emitter and 0.5% for a selective emitter process, according to the calculations presented in figure 11. Then, the efficiency gain of a selective emitter is approximately 0.2% compared to an industrial type homogeneous emitter.

5. CONCLUSIONS

In this study, selective diffusion barriers have been used to prepare selective emitters. This process has major advantages over other processes, most importantly the ease of control of emitter selectiveness. Crucial is the alignment of screen-printing the barrier layer and the front side metallisation. Inline production equipment is available for at high production volumes of 1000 wafers per hour for both aligned printing and surface passivation. This makes selective emitter produced by diffusion barriers a process suited for large-scale production.

Experimentally, selectivity has been confirmed and lightly doped sheet resistances have been varied between 50 and 100 ohm/sq. The produced selective emitter cells showed an increase in current of 2%, an increase in voltage of 1%, and increase in blue IQE response by a factor of 2. A decrease in fill factor reduces the efficiency gain to 1% (relatively). This loss can be partly attributed to the increase in emitter sheet resistance. Contact resistance scans show that fill factor losses occur due to a very localised high contact resistance. This can be solved by improved process control.

PC1D simulations show that the SiN_x provides some surface passivation. This SiN_x is optimised for mcSi solar cell efficiency, including bulk and surface passivation, short wavelength transmission, and anti-reflection. The simulations show that when bulk passivation and short wavelength transmission can be maintained, further gains will be possible with improved surface passivation.

For future research, the challenge is to combine the bulk and surface passivating qualities of the SiN_x.

ACKNOWLEDGEMENT

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REFERENCES

[1] S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, 1981.
[2] R.R. King et al, IEEE Trans. on Elect.Dev., Vol 37, No 2, pp. 365-371, 1990
[3] K.A. Münzer, K.T. Holdermann, R.E. Schlosser, S. Sterk, Proc. 16th EPVSEC, Glasgow, 2000, pp 1185-1188.
[4] J. Szlufcik, J. Horzel, F. Duerinckx, R. Einhaus, E. Demesmaeker, J. Nijs, and R. Mertens, Proc. 8th workshop cSi-solar cell materials and processes, Copper Mountain, 1998.
[5] J.H. Bultman, R. Kinderman, M. Koppes, J. Hoornstra, Proc. 16th EPVSEC, Glasgow, 2000, pp 1424-1426.
[6] M.J.A.A. Goris, H.H.C.de Moor, A.W.Weeber, E.J. Kossen, H.G. ter Beeke, L. Frisson, J. Szlufcik, Proc. 2nd WCPVSEC, Vienna, 1998, pp 1523-1526.
[7] M..J.A.A. Goris, A.W. Weeber, W. Jooss, F. Huster, Proc, 17th EPVSEC, Munich, 2001
[8] W.J. Soppe, Proc. 16th EPVSEC, Glasgow, 2000, pp 1420-1423.
[9] R.A. Sinton, A. Cuevas, Proc. 16th EPVSEC, Glasgow, 2000, pp 1152-1155.
[10]M.A. Green, Solar Cells, UNSW Press, 1998
[11]A.S.H. van der Heide, J.H. Bultman, J. Hoornstra, A. Schönecker, Proc, 17th EPVSEC, Munich, 2001
[12]P.A. Basore, D.A. Clugston, Proc. 25th IEEE PV Specialist Conference 1996; 377-381.
[13]M.J. Kerr, J. Schmidt, A. Cuevas, J.H. Bultman, J. Applied Physics, Vol. 89-7, pp 3821-3826, 2001
[14]A.G. Aberle, Crystalline Silicon Solar Cells: Advanced Surface Passivation and Analysis, UNSW Press, 1999
[15]J. Schmidt, M.J. Kerr, Sol. En. Mat. & Solar Cells, 65, 2001, pp 585-591