

LOW-TEMPERATURE METALLIZATION FOR CURRENT COLLECTION AND MONOLITHIC SERIES INTERCONNECTION OF FLEXIBLE THIN-FILM PV DEVICES

J. Löffler^{*1}, M.C.R. Heijna¹, E. Rubingh², T. van Lammeren², F. Furthner², R. Abbel², E.R. Meinders²,
M. Grouchko³, A. Kamishny³, S. Magdassi³, P.P.A.C. Pex¹

^{*}Corresponding author, phone +31 (224) 56 4421, e-mail: loffler@ecn.nl

¹ECN, Solar Energy, P.O. Box 1, 1755 ZG Petten, The Netherlands. ²Holst Centre, PO Box 8550, 5605 KN Eindhoven, The Netherlands. ³Casali Institute of Applied Chemistry, Edmond Safra Campus, The Hebrew University of Jerusalem, Jerusalem 91904, Israel

ABSTRACT: In the EU-FP7 project LOTUS an inkjet printing platform is developed including ink formulations and fast curing processes at low substrate temperature. This metallisation process is aimed for device fabrication by cost-effective roll-to-roll production. Here, the specifications of metallisation patterns for different thin-film silicon and organic photovoltaic (OPV) devices on flexible substrates are presented, together with a benchmark of existing screen printing and inkjet technologies using low-temperature curing silver inks and with first results from nanoparticle inks developed in the project. For the screen printing of narrow lines it is concluded that polymeric thin-film pastes achieve better aspect ratios, while nanoparticle based Ag formulations have proven the potential to approach the bulk conductivity of metallic silver. Commercially available inkjet formulations are comparable to these screen printed nanoparticle pastes. Finally, Ag inks with competitive conductivity potential that can be cured even at room temperature are presented as an example of promising solutions that are studied in the LOTUS project.

Keywords: Flexible substrate, Metallization, Thin-Film Solar Cell

1 INTRODUCTION

Roll-to-roll production facilitates the fabrication of flexible PV modules and a significant decrease of production cost e.g. for thin-film silicon and OPV solar cells. However, monolithic series interconnection on flexible foil substrates, and the application of current collecting metal structures, which are prerequisites for capturing the full potential of these PV technologies, are not straightforward. Printed metal patterns using low-temperature curing inks are required, and optimum combinations of ink, printing process, device structure and substrate have to be established.

While the printing materials and processes discussed here are generally applicable to all thin-film PV technologies and eventually also for crystalline silicon wafer based devices, we focus the description on the PV technologies that are explicitly taken as reference devices for the project, thin-film silicon and organic PV (OPV). ECN is currently developing the technology and setting up a pre-pilot line for the production of single junction and tandem solar cells based on microcrystalline and amorphous silicon on steel foil substrates. To allow monolithic series interconnection on these electrically conducting substrates, an insulating layer is required. In the presented module concept (see Figure 1), first all layers of the solar cell are deposited. After that series interconnection can be realized in one process step by three depth-selective laser scribes (P1, P2, and P3) which are then filled by insulating and electrically conductive inks.

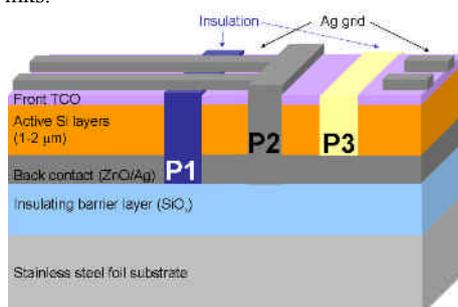


Figure 1. ECN Thin-Film-Silicon module concept.

In addition to achieving a monolithic series interconnection, the Ag grid also serves as current collector, requiring low line resistance combined with minimal shading losses. As an alternative to monolithic modules, cost-effective wafer equivalent solar cells can be manufactured by thin-film technology, with similar current collecting grids as crystalline silicon solar cells.

Similar structures as for TF-Si are studied for OPV, see for example Figure 2. Note that the results presented in this paper are also relevant for advanced honeycomb metallization as recently applied for 'ITO free' OPV devices [1].

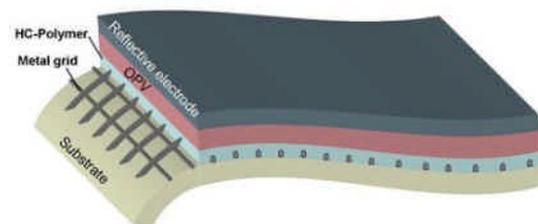


Figure 2. Example of an OPV device on flexible substrate with printed metal grid.

At present, no standard high-throughput roll-to-roll processes for low-temperature curing printed metallisation of PV devices on flexible foil substrates are readily available. In the EU-FP7 project LOTUS an inkjet printing platform is developed including the ink formulations and fast curing processes as building block for future device fabrication. In general, inkjet printing has the advantage of a flexible, non-contact, digital technology compatible with nanoparticle formulations that promise very high conductivity in combination with low curing temperatures. The height of the printed features however is limited to about 600 nm per pass. Screen printing, in contrast, offers a proven technology for PV metallization enabling relatively high aspect ratios for narrow lines with feature height of more than 10 μm.

In this contribution, the specifications of metallization patterns for different thin-film silicon and

organic photovoltaic (OPV) devices on flexible substrates are presented, together with a benchmark of existing screen printing and inkjet technologies using low-temperature curing silver inks and with first results from room temperature sintering nanoparticle inks developed in the project.

2 EXPERIMENTAL

2.1 Device simulations

In order to establish the specifications for the metallization, the electrical losses in the PV devices have been simulated with the software PatOpt [2], which was originally designed for the modeling of crystalline silicon solar cells with so-called H-pattern metallization, consisting of narrow gridlines and (typically 2) wider busbars. The simulation of a device like depicted in Figure 1 including the monolithic interconnection - being a dead area - can be incorporated into PatOpt by choosing the width of the busbar to be twice the width of the dead area. The result is a $0.5x$ by $2x$ cell with the interconnection dead area on one side of the cell instead of a square x by x H-pattern with one busbar (see Figure 3). This only holds when the tab resistance is set to zero. A small error is introduced as the silver fingers in the thin film interconnection scheme are printed over the insulating paste and thus extend into the dead area. In the PatOpt simulation, the fingers end at the edge of the dead area. From that point onwards resistance is set to zero. Thus, the fingers are approx. $100\ \mu\text{m}$ shorter than in the actual thin film configuration. The larger the cell size, and thus finger length, the smaller is the influence of this error.

As input IV data typical values for amorphous silicon single junction cells and amorphous-microcrystalline tandem solar cells in nip configuration are taken from literature [3][4].

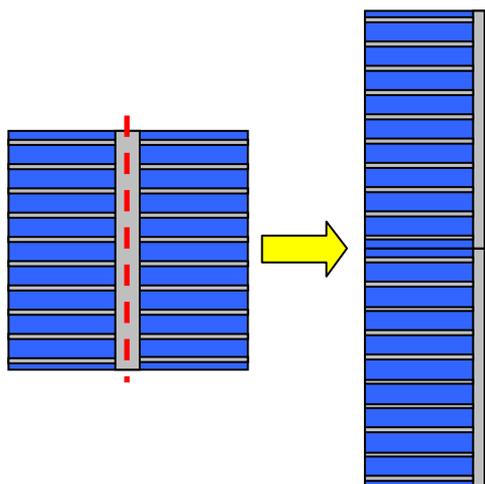


Figure 3. Schematic representation of cutting up an x by x H-grid pattern into a $0.5x$ by $2x$ thin film pattern. The red dashed line indicates the cutting line.

2.2 Screen printing

The screen printing experiments were conducted on a semi-automatic EKRA printer. Besides the printing parameters, also screen properties like mesh and emulsion were varied to achieve optimal results.

Substrates allowing easy characterization of the lines like glass and polymers have been used, as well as ITO as a specific surface that is relevant for the final devices. Several commercially available inks based on different approaches to achieve low curing temperatures, such as polymeric thick-film pastes and nanoparticle pastes have been tested.

2.3 Inkjet printing

A FujiFilm Dimatix Materials Printer (DMP 2831) with 10 pL cartridge was applied for the inkjet experiments with SunTronic U5603 ink (20-40 wt% Ag). The drop spacing was set at $20\ \mu\text{m}$, resulting in 50 pixels/mm. The lines were cured in a box oven at 190°C for 15 min. For multiple-pass printing, a 1 minute drying step at 190°C was introduced between the printing passes.

2.4 Analysis of printed structures

The resistance of the printed lines has been measured with standard 4-point technique. Contact resistances were determined from 4-point measurements on TLM structures. The line shape was determined by 3-d profilometry (Microvison) and in some cases with a DekTak stylus profilometer. The metal fill factor MFF is determined as the ratio of the measured cross section and the ideal cross section of a line with rectangular shape (calculated as product of height and width of the line).

3 RESULTS AND DISCUSSION

Starting from the described thin-film silicon and OPV devices, the requirements for current collecting and interconnecting metallization structures have been deduced, supported by simulations of resistive losses in these devices. In a next step Ag lines have been prepared by screen printing and inkjet printing including a new formulation developed in the LOTUS project.

3.1 Specifications

Thin-Film Silicon

In first instance, monolithically series connected devices like depicted in Figure 1 have been considered, and realistic parameters to achieve collection and interconnection losses due to the metallization in the order of 10% were determined. Then, all parameters have been varied in PatOpt within reasonable windows in order to come to a range of acceptable specifications enabling overall series interconnection losses below 10%. Table 1 summarizes the findings, together with specifications due to restrictions and demands from the used materials, other processing steps, and the final devices. In the following, a more detailed discussion of these specifications is presented.

For the sheet resistance a benchmark value of $25\ \text{m}\Omega/\square$ follows from previous experimental results [5]. Based on the calculations using the PatOpt program, a maximum of $50\ \text{m}\Omega/\square$ is chosen as a guideline. Specifications for resistivity and line height are not specified, as long as the sheet resistance of the printed line is achieved.

Line widths of $50\ \mu\text{m}$ have been achieved before [5]. PatOpt calculations show that lines in the range of 50 - $100\ \mu\text{m}$ are required to have an optimum between resistance losses and shadow losses. An upper limit of $150\ \mu\text{m}$ is set as a typical industrial achievable size.

Apart from the resistance of the printed lines and the TCO on the front side of the solar cell, the contact resistance between line and TCO has to be taken into account. Varying the contact resistance in a realistic range, we found a significant influence on the losses in the PV devices (see Figure 4), and based on PatOpt the maximum contact resistance is set in the order of $50 \text{ m}\Omega \text{ cm}^2$.

Table 1. Requirements for metallization of Thin-Film Silicon devices.

	min	max	unit
Sheet Resistance	-	50	$\text{m}\Omega/\text{sq}$
Resistivity	see R_{\square}	see R_{\square}	Ωm
Structure height (dry)	see R_{\square}	see R_{\square}	μm
Minimum line width	50	150	μm
Contact Resistance	-	50	$\text{m}\Omega \text{ cm}^2$
Substrates	ITO, ZnO, Ag, a-Si, insulation paste		
Surface Roughness	0.15		μm
Adhesion	scotch 610 tape 4 cm		
Sinter/Fuse temperature	-	200	$^{\circ}\text{C}$
Maximum sinter time @ T_s	-	10	min
allowed temp. after sintering	150	-	$^{\circ}\text{C}$
print over isolation line	5	-	μm

The substrates to print the silver lines onto are all layers in the thin film silicon solar cell. The main material onto which is printed is the front TCO (ITO). In the laser scribes, the other layers may be exposed to the printing ink.

An insulating paste is printed into one of the scribes (P1). The silver lines need to be printed over these lines. The insulating paste is an approximately $5 \mu\text{m}$ high line, and the electrical connection over this line is to remain intact (i.e. no discontinuation of the silver line due to the height difference).

The surface of the solar cell may be textured as a result of texturing for light trapping. Typically, the surface roughness of such a textured surface is in the order of $150 \text{ nm } R_a$. Peak-to-valley differences can range up to 300 nm .

The adhesion of printed lines is tested by a standard tape test. The lines should not come off the substrate when removing tape with a peel strength in the order of $15 \text{ N}/100 \text{ mm}$ width. Next to that, the lines should withstand bending of the substrate/solar cells down to a radius of 4 cm which may be required during manufacturing.

The maximum temperature to be used for sintering is 200°C ; materials used in the substrate can handle this temperature, and the silicon should not be annealed at temperatures higher than the deposition temperature. Sinter time is mainly limited by cost (longer is more expensive) and by potential degradation of the solar cell. Due to the elevated temperature during sintering, the dopants in the doped silicon can diffuse into the intrinsic silicon and thus degrade the device structure.

After printing and sintering, the solar cell needs to be encapsulated to protect it from climate influences. A standard technology is lamination with EVA at 150°C . Thus, the sintered lines should be able to handle a temperature of at least 150°C . Demands for encapsulation

compatibility may change with the development of new encapsulation methods.

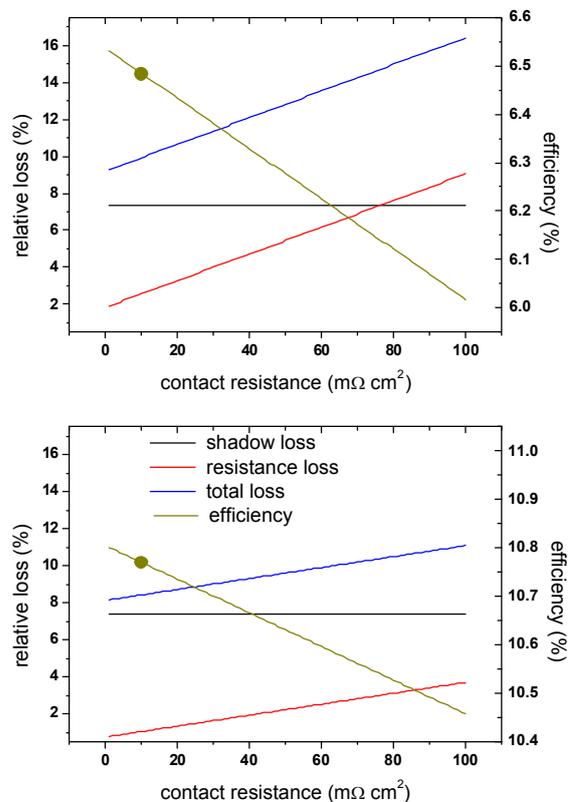


Figure 4. Calculated losses for amorphous single junction (top) and amorphous/microcrystalline tandem modules (bottom) as function of contact resistance between front TCO and printed Ag.

OPV

As described above, very similar considerations are valid for OPV devices. The main additional requirements are the even lower temperatures that are allowed due to the organic materials and also polymer substrates that are often applied. The layers in organic PV are typically quite thin, and thus smooth surfaces are required to prevent shunting of the solar cells. Besides, for device structures where the grid lines are applied directly onto the substrate before coating with the active solar cell layers, the gradients of the line should be small and/or the line height below $1.5 \mu\text{m}$ to avoid too sharp steps. A summary of the specifications for OPV metallization is given in Table 2.

Table 2. Requirements for metallization of OPV devices.

	min	max	unit
Resistivity	$1.60\text{E-}08$	$8.00\text{E-}08$	Ωm
Structure height (dry)		1.5	μm
Minimum line width	50	150	μm
Contact Resistance	0.4	50	$\text{m}\Omega \text{ cm}^2$
Substrates	ITO, hc-PEDOT, ZnO, TiO_2 , barrier film,		
Surface Roughness	10		nm
Sinter/Fuse temperature	130		$^{\circ}\text{C}$
Maximum sinter time @ T_s	1		min
allowed temp. after sintering	90	130	$^{\circ}\text{C}$

3.2 Screen printing

The results of a first screening of different low-temperature curing Ag pastes and the optimization of their printing and curing processes can be seen in Figure 5.

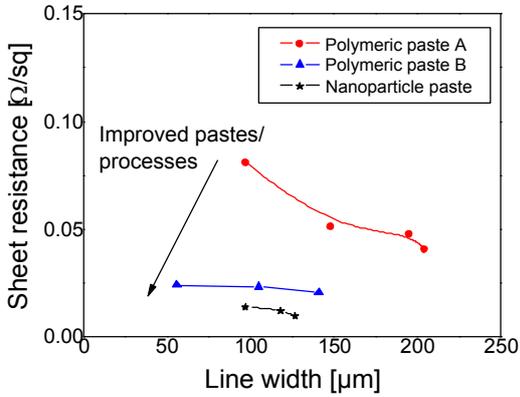


Figure 5. Sheet resistance of screen printed narrow silver lines from low-temperature curing pastes as function of the line width.

Commercially available polymer-containing inks achieve ~ 25 mΩ/sq and thus approach the performance necessary to reduce interconnection losses below 10%. Taking into account also the line heights, which we determined between 5 μm for the nanoparticle paste up to 15-20 μm for the best polymeric pastes, the bulk resistivity can be estimated. Typical values for bulk resistivity of polymeric paste after curing at moderate temperature below 200°C is in the order of 10 times the resistivity of metallic silver, while nanoparticle pastes can enter into the region < 3-5 times metallic silver resistivity. The nanoparticle paste tested here however had issues with adhesion to the relevant surfaces, therefore in the following the best polymeric paste was used as baseline to have a benchmark reference for the inkjet materials and processes.

Figure 6 nicely illustrates the virtually constant metal fill factor with decreasing line width, confirming a robust line profile, which also explains the constant sheet resistance as observed in Figure 5.

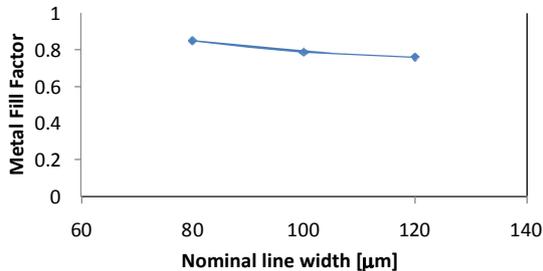


Figure 6. Metal fill factor for screen printed lines with polymeric paste as function of line width.

Typical contact resistance values on representative ITO samples range between 10 and 30 mΩcm², and thus meet the specifications as presented above.

3.3 Inkjet printing

In contrast to screen printing, a single printing step with the applied inkjet printer and ink resulted in line heights between 200 and 600 nm only, see Figure 7

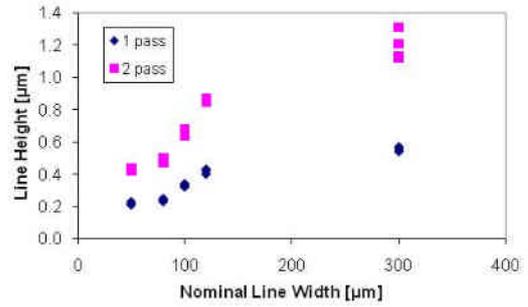


Figure 7. Line height as function of line width for inkjet printed lines.

The resulting electrical properties of lines printed in a single pass and in 2 passes are shown in Table 3.

Table 3. Electrical properties of inkjet printed lines in single and double pass.

Nominal line width (μm)	Sheet resistance (mΩ/sq)			Resistivity (×10 ⁻⁸ Ω m)		
	1 pass	2 passes	Screen print ref.	1 pass	2 passes	Screen print ref.
300	231	112	15.7	12.7	10.6	27.7
120	228	148	15.2	12.5	10.5	26.9
100	314	178	21.7	13.2	8.6	17.6
80	381	230	26.5	12.6	7.6	20.2
50	486	288	31.3	11.7	7.4	21.5

The resistivity of the inkjet printed lines is 5 times lower than that for the screen printed lines, but due to the low height of the lines, the sheet resistance is more than one order of magnitude higher. It is also observed that the sheet resistance increases with lower line width. As the metal fill factor is virtually independent of the line width (see Figure 8), the variation in sheet resistance is mainly attributed to height variations.

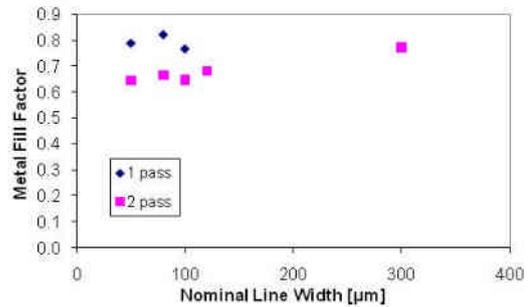


Figure 8. Metal fill factor as function of line width for inkjet printed lines.

Recently, more efforts have been undertaken to print higher lines up to 5-10 μm. So far, 5 to 10 passes with intermediate drying have been applied, leading to sheet resistance values around 30 mΩ/sq, comparable to the values obtained for the screen print baseline already at significantly lower line height. Also the contact resistance to ITO achieves already the specifications (typically 40-60 mΩcm²). Further research will be conducted towards inkjet printing of higher lines with good definition and high

metal fill factors, aiming at lines with lower sheet resistance compared to the polymer based screen printing baseline. Besides, materials will be developed with lower resistivity than commercially available, and focus will also be laid on fast curing at low temperatures.

As an example of the materials and technologies that are developed and studied in the LOTUS project, a new approach to achieve sintering of metallic nanoparticles at room temperature [6] is presented here. It was discovered that silver nanoparticles behave as soft particles when they come into contact with oppositely charged polyelectrolytes and they undergo a spontaneous coalescence process, even without heating. Utilizing this finding in printing conductive patterns, which are composed of silver nanoparticles, enables achieving high conductivities even at room temperature. Because of the sintering of nanoparticles at room temperature, the formation of conductive patterns on plastic substrates (PET) is made possible. Already first results on polymeric substrate with bulk conductivities of ~ 20% bulk Ag conductivity demonstrate the potential of this technology.

4 SUMMARY AND CONCLUSIONS

In the EU-FP7 project LOTUS an inkjet printing platform is developed including ink formulations and fast curing processes at low substrate temperature. This metallization process is aimed for device fabrication by cost-effective roll-to-roll production. Here, the specifications of metallization patterns for different thin-film silicon and organic photovoltaic (OPV) devices on flexible substrates are presented, together with a benchmark of existing screen printing and inkjet technologies using low-temperature curing silver inks and with first results from nanoparticle inks developed in the project. While polymeric thin-film pastes for screen printing achieve better aspect ratios, nanoparticle based Ag formulations have the potential to approach the bulk conductivity of metallic silver. A novel approach to room temperature sintering of inkjet-compatible nanoparticles is presented. In general, inkjet printing has the advantage of a flexible, digital technology, while screen printing so far enables higher lines to be printed.

ACKNOWLEDGEMENTS

This work was partially financed by the European Commission under FP-7-ICT-2009-4, grant agreement 248816 (LOTUS project).

REFERENCES

- [1] R. Andriessen *et al.*, this conference (1DO9.3).
- [2] Patopt, optimising H-grid patterns with patopt program. Author: A.R. Burgers, ECN, The Netherlands.
- [3] K. Brecl, M. Topič, *Progr. in PV Res. and Appl.* 16 (2008) 479-488.
- [4] T. Söderström *et al.*, *J. Appl. Phys.* 107 (2010), 014507.
- [5] Löffler *et al.*, *proc. 23rd EUPVSEC*, 2008.
- [6] S. Magdassi *et al.*, *ACS Nano* 4(4) (2010) 1943-1948.