INNOVATIVE DIFFUSION PROCESSES FOR IMPROVED EFFICIENCY ON INDUSTRIAL SOLAR CELLS BY DOPING PROFILE MANIPULATION

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ABSTRACT: Manipulation of the doping profile of phosphorus emitters in silicon solar cells is demonstrated in an industry-applicable process. By changing the diffusion temperature—time (T-t) curve without increasing process time, the surface phosphorus concentration has been reduced resulting in an efficiency gain of 0.2% absolute. In addition, batch quartz tube furnace with gaseous dopant source and inline conveyor furnace with liquid dopant source were fairly compared by introducing an artificial process recipe with an identical T-t curve for each furnace. This comparison shows that the open circuit voltage is independent of the diffusion furnace type. This suggests that crucial factor regarding emitter quality is a lower process temperature and increased process time rather than diffusion furnace choice.
Keywords: diffusion, doping profile, process control

1 INTRODUCTION

Emitter quality is crucial for good solar cell performance. However, regarding emitter improvements, the PV industry has focused lower process costs and increasing furnace throughput. Emitter diffusion is the most time-consuming process step in solar cell manufacturing. Therefore, improving emitter quality should not lead to longer process times. Our solution to this dilemma is to manipulate the doping profile without longer diffusion time by introducing multi-temperature plateaus.

In parallel, we have investigated the intrinsic difference in the emitter performance between the two major types of phosphorus diffusion tools: batch type quartz tube furnace with gaseous dopant source and inline conveyor furnace with liquid dopant source. So far, several review articles modestly discussed the difference [1-3], but these comparisons were made with the emitter quality at the minimum-necessary level and the throughput as high as possible. We introduced an artificial process recipe for each tool which enables a fair comparison between batch and inline based on device performance.

2 APPROACH

Although the main focus has been on improving throughput rather than performance, some approaches have been presented to improve the emitter performance. A typical example is "selective emitter" where phosphorus is highly doped under the metal finger contact and lowly doped under the anti-reflective coating (ARC) [4-6]. This requires another process step in addition to the primary diffusion step or multiple other processing steps, which normally results in a large increase in total processing time. It is always controversial whether the performance improvement can compensate the increased cost caused by the additional processing steps.

Another approach is doping profile manipulation of the phosphorus emitter. It was reported on laboratory scale as so called “passivated emitter” concepts (*i.e.* PERL concept, Univ. of New South Wales [7]). These emitters show very high internal quantum efficiency (IQE) in the short wavelengths, suggesting that higher efficiencies are feasible. This structure can also be categorized as selective emitter, and it has a drawback that two or three (or even more) heating processes with wet chemical processes in-between are required. Speculating from the cell performances, we estimate that the emitter doping profile must have a very low surface concentration around $1 \sim 3 \times 10^{19}$ /cm³ with an excellent surface passivation due to a thermal oxide. It suggests that reducing the surface phosphorous concentration is a key in improving emitter performance.

Normally, only one heating process is allowed for industrial emitter process to not increase the cost of ownership. It is not possible to realize a PERL-like emitter profile with a single heating process unless one can deposit extremely small amount of phosphorus with precise control. Figure 1 shows the simplified drawing of the phosphorus emitter profile formed with a single heating process. The diffusivity of phosphorus ($D_{[P]}$) at the phosphorus concentration ([P]) of 1×10^{19} /cm³ is 5 ~ 7 times larger than the $D_{[P]}$ at [P] = 1×10^{20} /cm³ [8]. Therefore two Gaussian-like curves appear: one starts at the surface and the other starts at [P] ~ 3×10^{19} /cm³. This causes the formation of two different layers with different [P], which are called n^{++} and n^{+} layers from now on.

The existence of the n^{++} layer has both positive and negative effects. The major positive effect is that it enables a good contact with silver print paste with relatively low resistance, which simplifies the industrial production process. One of the negative effects is that the heavily-doped phosphorus in the n^{++} layer results in an increased carrier recombination, yielding a lower

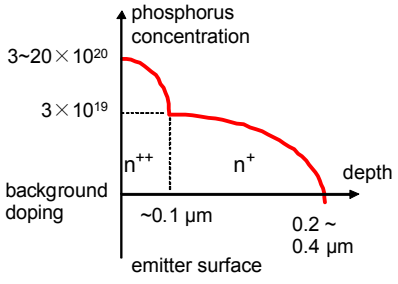

Fig. 1: Simplified model of phosphorus doping profile formed by industrial emitter formation process.

operating voltage of the solar cell. We speculate that a well functioning "passivated emitter" on laboratory scale will not have an n^{++} layer because of its very high V_{oc}. An n^{++} layer is required for screen-printed solar cells in order to form a good contact with the silver contacts. But it should have low [P] and/or shallow depth to minimize carrier recombination. It is contradicting to aim at both a higher voltage and a better contact simultaneously, and the best compromise can be reached by optimizing the n^{++} layer.

The role of the n^{+} layer is more evident: it forms a pn-junction with the base p-type wafer. Although a too deep n^{+} layer may have a negative effect for the photo-generated current, a certain depth is required to secure sufficient lateral conductivity for electrons as the majority carrier in this layer.

Concluding these scopes for n^{++} and n^{+} layers, the direction of improving industrial emitters should be toward a shallower n^{++} layer with lower doping to minimize carrier recombination, and a deeper n^{+} layer to compensate for the loss in lateral conductivity in the n^{++} layer.

3 DOPING PROFILE MANIPULATION

3.1 Direction of manipulation

Figure 2 shows a phosphorus doping profile characterized by SIMS (secondary ion mass spectroscopy) with an active dopant profile by ECV (electrochemical capacitance voltage). The doping layer has been formed by a process recipe typically used in production. In order to measure the profile accurately, a polished CZ wafer was used. The diffusion tool used was an industrial scale $POCl_3$ tube furnace, equipping 400 slots for loading 156×156 mm² wafers in its temperature-flat zone (Tempress TS81003).

The two measured profiles agree with each other where [P] < 3×10^{20} cm³ if the measurement error in depth is ignored. This suggests that excess phosphorus atoms are present where [P] > 3×10^{20} cm³ in the n^{++} layer. These atoms are electrically inactive and prone to behave as SRH (Shockley-Read-Hall) recombination centers. An improvement of the emitter performance is to be expected if the concentration of these inactive phosphorus atoms in the n^{++} layer can be reduced,

3.2 Process control

It is possible to manipulate the doping profile without increasing process duration by changing temperature in

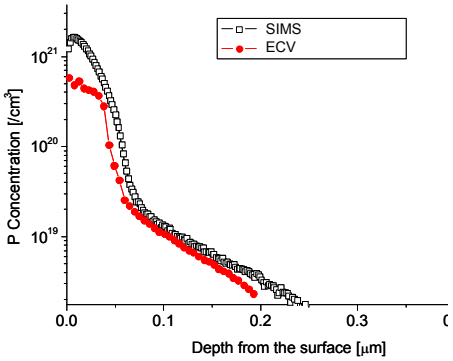

Fig.2: SIMS and ECV profiles of an emitter layer formed by a POCl3 tube process recipe typically used in production.

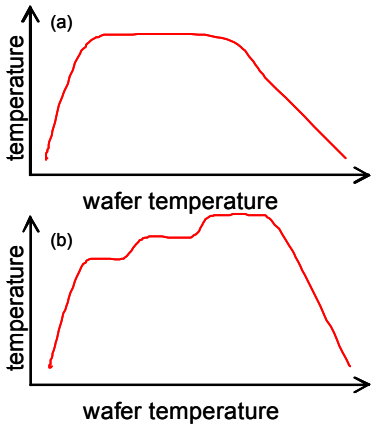

Fig.3 : (a) Typical temperature time (T-t) curve with single temperature plateau carried out at the industrial production lines. (b) T-t curve example with multiple plateau.

the temperature - time (T-t) curve. Fig. 3(a) depicts a typical T-t curve as used in industrial production. It has a single temperature plateau at which all processes take place. In this study, we have introduced several process recipes with different T-t curves, all having multiple and different temperature plateaus in order to diversify the n^{++} profile. These process recipes were tuned to have equivalent sheet resistances to excluded differences in lateral conductivity. Table I shows the average sheet resistance of the emitters formed on acid-textured mc-Si obtained with the process recipes employed in this study.

3.3 Doping profile

Figure 4 shows the phosphorus doping profiles characterized by SIMS of these four types of emitters on polished CZ wafers. Compared to single plateau T-t emitters, the [P] at the n^{++} layer was successfully reduced due to multiple-plateau T-t curves. At the same time, the n^{+} layer is diffused deeper. The deeper n^{+} layers of multi-plateau T-t curves explain that the increase of the majority carrier conductivity of the n^{+} layer compensates its decrease in the n^{++} layer although the doping profile on textured mc-Si may not be completely identical to those on CZ,

3.4 Cell I-V characteristics and discussion

Mc-Si solar cells were produced in ECN's semi-industrial production line using the above described emitters. The size of the wafers is 156 × 156 × 0.2 mm³. Each group consists of 26 wafers, except group "multi B" which was just tested with small group of 6 wafers, with distributing neighboring wafers to each emitter process group. Figure 5 shows average I-V characteristics of the produced cells of each group, plotted statistically as means with 95% honestly significant difference (HSD)

Table I: Average sheet resistance on textured ms-Si obtained with the process recipes in this study.

T-t curve	Sheet resistance
Single plateau (reference)	66 ohm / sq
Multi plateau A	66 ohm / sq
Multi plateau B	59 ohm / sq
Multi plateau C	71 ohm / sq

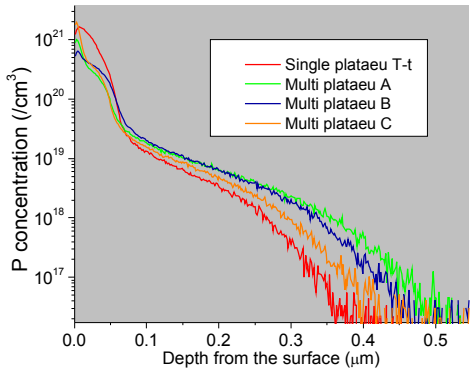

Fig. 4: SIMS profiles of doping layers formed by diversified process recipes with different T-t curves.

intervals.

The group "multi C" shows efficiency gain of 0.2% compared to the group "single". Also the group "multi A" shows a slight efficiency gain (~0.1%) compared to "single". Both groups A and C have J_{sc} gain of 0.3 ~ 0.4 mA/cm², and all "multi" groups have V_{oc} gain of 3 ~ 6 mV. V_{oc} is improved for the groups "multi" due to the reduction of [P] in the n^{++} layer (see Fig. 4). "Multi A" has the highest V_{oc}, which may be caused by both low surface [P] and shallow n^{++} layer.

The benefit of a high surface [P] on the contact between emitter and the Ag metal contact is clear from the differences in FF: the FF of "multi C" is equivalent with that of "single" while that of "multi A" is over a percent lower. Figure 4 illustrates that "multi C" has higher surface [P] than "multi A".

An efficiency gain is hardly seen for "multi B". The reason is not cleard yet mainly because the number of tested wafers is small. However, it suggests that successfully-looking doping manipulation does not always lead to an efficiency gain.

We have demonstrated that it is possible to manipulate the doping profile in simple ways with an industrial type furnace and process, resulting in efficiency improvement by 0.2% absolute.

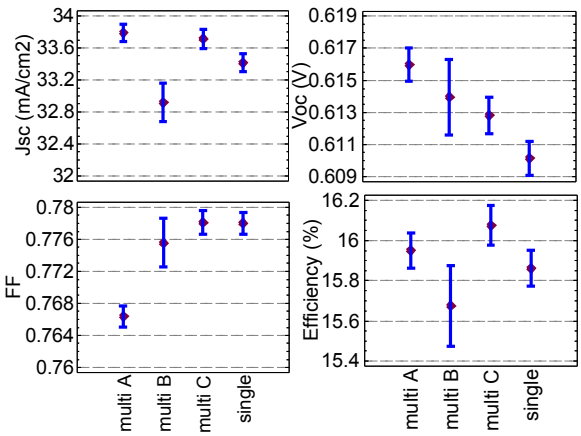

Fig. 5: Statistic plots of I-V characteristics of mc-Si solar cell for each emitter process group, produced using ECN's semi-industrial production line with distributing neighbouring wafers to each emitter process group

4 COMPARISON INLINE AND BATCH

4.1 Process tuning policy in industry

There has been a long-time debate in the PV industry concerning the question which tool is intrinsically better for the emitter process, inline conveyor furnace or batch tube furnace.

The main differences can be summarized as shown in Table II [1]. Among the several subjects, process duration per wafer is prominent on the point of view of process design. What enables shorter process time for inline conveyor furnace is its open-air chamber concept which does not require replacement of the hazardous gas inside. The typical process duration normally used in the PV industry is designed to be as short as possible, mainly taking into account process duration; emitter quality is of less importance.

In the case of the batch tube furnace, although shorter process duration is desired as well, the total process time remains relatively long because waiting time is required by such factors as temperature stabilization throughout the heat zone; distributing diffusion precursor throughout the chamber; and purging out hazardous gas before taking out the wafers. Since the purging of the hazardous gas occurs at elevated temperatures, the diffusion of phosphorus continues during this step, resulting in a further lowering of the sheet resistance. Therefore for obtaining identical sheet resistances, the process temperature of the batch tube furnace is normally lower than that of the inline conveyor furnace in order to compensate for the longer diffusion time.

4.2 Process parameters for fair comparison

Fair comparison for the intrinsic difference between inline and tube furnaces should meet the condition that the following three parameters should be identical: the process temperature, the duration from start to end of the phosphorus diffusion phenomenon, and the consequently obtained sheet resistance. Thus far, it requires artificial recipes for both furnaces.

In this study, we employed a basic T-t curve with a single plateau as shown in Fig. 6. As a starting point, the duration $t_{plateau}$ is defined from the limitations of the tube, such as purging of hazardous gas before taking out wafers and securing sufficient diffusion uniformity within a wafer. It is shorter than the normal $t_{plateau}$ (*e.g.* employed in Table I) while it is sacrificing the diffusion

Table II: Brief summary of the differences between inline conveyor furnace and batch tube furnace [1]

Furnace type	Inline conveyor	Batch tube
Process duration per wafer	20 ~ 40 minutes.	1 ~ 2.5 hours.
Way to apply phosphorus on Si wafers	As liquid on cold wafers, which enables open chamber.	As vapor on hot wafers, which requires semi-closed chamber.
Wafer loading	Horizontal.	Vertical.
Solutions for larger throughput	Wider belt. Longer belt with higher speed.	Longer tube. Back to back loading. More tubes stack on top.

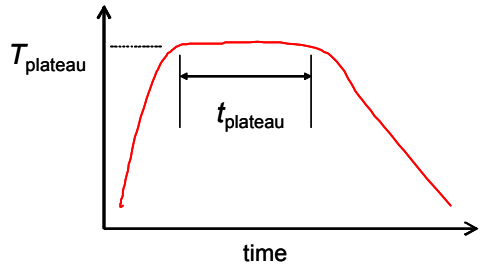

Fig. 6: T-t curve employed to make fair comparison between inline and tube furnaces.

Table III: Process parameters for reference and artificial recipes to make fair comparison between inline and tube furnaces

Group & Furnace	$T_{plateau}$	$t_{plateau}$	R_{sheet} and standard dev. (ohm/sq.)
Inline ref	T_{inline}	t_{inline}	58 ± 1.2
Inline comp.	T_{comp}	t_{comp}	58 ± 1.6
Tube comp.	T_{comp}	t_{comp}	58 ± 2.0

$t_{comp} = 2.1\ t_{inline}$: Minimum duration for purging out and uniform diffusion required for the tube furnace.

$T_{comp} = T_{inline}$ - 18ºC : Temperature defined by tuning to realize identical sheet resistance with "inline ref" group at the duration t_{comp} for both inline and tube furnaces.

homogeneity throughout the diffusion chamber of the tube because of insufficient distribution of the diffusion precursor.

ECN's standard process, which uses the inline conveyor furnace for the emitter diffusion process, was defined as the reference group in this comparison. Its R_{sheet} is 58 ohm/sq., and the process parameters of plateau temperature and plateau time are defined as T_{inline} and t_{inline}, respectively. The plateau time for the artificial recipe t_{comp} was defined as 2.1 t_{inline}, considering the factors described above. By tuning both the inline and the tube furnaces toward R_{sheet} = 58, the plateau temperature for the artificial recipe T_{comp} was found to be 18ºC lower than T_{inline}. Process parameters are summarized in table III.

4.3 Cell I-V characteristics and discussion

Mc-Si solar cells were produced using ECN's semi-industrial production line with distributing neighboring wafers to each emitter process group. Wafer size is 156 × 156 × 0.2 mm³ and each group consists of 25 wafers. Figure 7 depicts the cell I-V characteristics, plotted statistically as means with 95% HSD intervals.

Due to identical process temperature of the groups "inline comp" and "tube comp", the values of V_{oc} are statistically the same. However, the values of J_{sc} differ, whose reason is not cleared yet among several possibilities. The J_{sc} of the group "inline comp" is higher than that of the group "tube comp". The differences in FF among three groups are not statistically significant.

It is interesting that both J_{sc} and V_{oc} are higher in the "inline comp" than in the "inline ref". Since the artificial process differences only in the plateau temperature (lower) and the plateau time (longer) from the reference. One can say that by sacrificing the throughput of the inline conveyer furnace, an efficiency gain of at least 0.2% absolute can be obtained.

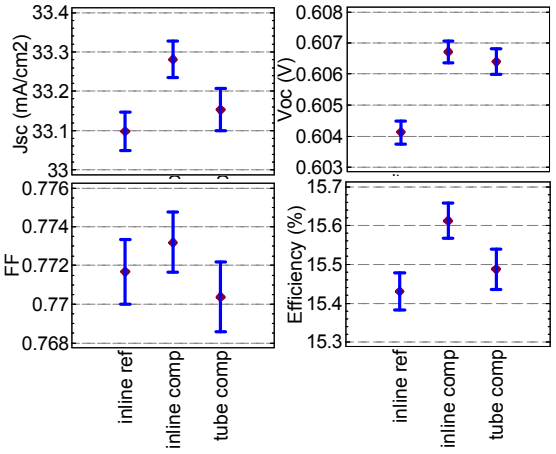

Fig. 7: Statistic plots of I-V characteristics of mc-Si solar cell produced by artificial recipes for fair comparison between inline and tube furnaces, with ECN's standard inline recipe as the reference.

The artificial recipe for the batch tube furnace resulted in a slightly lower performance than that for the artificial inline furnace recipe, and even lower than the standard industrial tube furnace recipe whose T-t curve has a plateau with still lower temperature and longer time.

From the observed trend we conclude that the crucial factor to improve the solar cell performance is to lower the plateau temperature with increased process time. Although certain parties in industry are of the opinion that batch tube diffusion results in higher efficiencies than the inline furnace, this is most likely just a result of the longer minimum necessary process duration per wafer of the batch tube compared to the inline conveyor. The inline furnace is often operated at its largest possible throughput capability, sacrificing potential efficiency gain. This is a good example of the dilemma between performance and throughput regarding diffusion process.

But independent of the diffusion tool, conversion efficiency can be improved by increasing process time and lowering diffusion temperature, as long as increased cost can be compensated by increased performance.

5 CONCLUSION

Manipulation of the phosphorus emitter doping profile is demonstrated in an industry-applicable process aiming at improvement of solar cell performance. By changing the T-t curve of phosphorus diffusion without increasing process duration —especially introducing multiple temperature plateaus—, phosphorus concentration in the n^{++} layer can be reduced, resulting in an improvement of the solar cell efficiency of 0.2% absolute.

In addition, a fair comparison between batch tube furnace and inline conveyor furnace was carried out, with the emphasis on efficiency and not throughput. An artificial process recipe for each furnace was introduced with identical T-t curve. V_{oc} of the cells diffused in the batch tube and the inline furnaces showed little difference, and the comparison with the reference groups shows once more that to improve the device performance, a lower process temperature combined with an increased process

time is required independent of choice of diffusion tool.

As a conclusion, two factors have been shown to improve the device performance at the emitter process: introducing multiple-plateau T-t curve and lower process temperature. Although the latter requires longer process duration, the extent will be minimized by combining the two.

ACKNOWLEDGMENT

This work is financially supported by the SenterNovem EOS-KT, project nr IS074007.

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