17.4% EFFICIENCY SOLAR CELLS ON LARGE AREA AND THIN N-TYPE SILICON WITH SCREEN-PRINTED ALUMINUM-ALLOYED REAR EMITTER

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ABSTRACT: We present results on n-type silicon cell process development based on large area and thin wafers with screen printed Aluminum-alloyed rear junction concept. An independently confirmed record-high efficiency of 17.4% (140 cm²) has been achieved on floatzone silicon wafers using simple and low cost fabrication techniques. Moreover, model calculations allow us to identify the potential for further enhancement of the cell efficiency towards 18.0% by improving front surface passivation. After some optimization, high efficiencies may be conceivable on n-type multicrystalline substrates as well.
Keywords: n-type solar cells, aluminum-alloyed emitter, rear junction.

1 INTRODUCTION

The vast majority of today's commercial silicon solar cells are made from p-type doped material. More than 80% of the produced solar cells have a homogeneous emitter, a PECVD-SiN layer as antireflective coating, and screen printed contacts on both sides. For the backside, an aluminum paste is used to create a back surface field during the contact co-firing. Recently, n-type silicon materials have received much interest as they are considered promising candidates for future generations of high-efficiency solar cells. This interest is based on several developments and findings, such as:

- High carrier lifetimes in n-type multicrystalline wafers, often significantly higher than in p-type wafers.
- Theoretical and experimental evidence for less recombination-active defects in n-type silicon [1].
- Tolerance of n-type silicon to high temperature processing with respect to p-type silicon [2].
- Shortage of silicon feedstock for the PV industry, and an unused potential supply of n-type silicon waste.
- New materials (ribbons, metallurgical feedstock) for which the above aspects favour n-type doping.
- Need for technology development towards very thin wafers and high cell efficiency, for which n-type silicon based solar cells, may have advantages.

However, in spite of these advantages, the n-type solar cells are not yet abundantly produced in industry. In order to realize this, n-type silicon solar cells must have stable efficiencies of at least the same level as for p-type.

A few solar cells concepts based on n-type Si materials are currently under investigation. One of these concepts is the Al-alloyed back-junction cell [3-10]. This concept was introduced for the first time by EBARA Solar Inc. in 2000 [9], and it represents a fast way, for industry, to move from p-type to n-type substrates because of the possibility of maintaining the same process sequence. The only difference, as compared with the conventional p-type (n^+pp^+) process, is that during the phosphorus diffusion a front surface field is created instead of an emitter and during the contact co-firing the aluminium back junction is formed. Triggered by a reduction in costs, wafer thickness in the industry is decreasing rapidly and it is becoming more important to develop all rear contacted solar cell processes. Aluminum rear-junction is an interesting and elegant approach to study and identify the material limitation for developing all back-contacted solar cells. In particular, this concept can be well used to study limitations of multicrystalline n-type substrates for high efficiency rear-emitter cell concepts.

Recently cell efficiencies up to 17.0% were reported for Al-alloyed rear junction cell concept [7]. In this paper we present results on our n-type cell development based on the Al back-junction. We present an independently confirmed new record-high efficiency of 17.4%, which demonstrates exceptional potential for high efficiency of n-type process. We present modelling showing possibilities and limitations for further improvements. We also focus on mc-Si substrates to study limitations of mc n-type wafers for high-efficiency rear-junction application.

2 EXPERIMENTAL PROCEDURE

The cell process is developed on 148.5 cm^2 Float Zone (FZ) n-type monocrystalline silicon wafers, but preliminary results on 156.25 cm^2 industrial n-type multicrystalline silicon (mc-Si) wafers are also presented in this paper. The cell process we used is based on in-line processing for diffusion, co-firing, and on process steps which can be industrialized. The rear junction as well as the front surface field (FSF), anti-reflection coating (ARC), and the metallization, are comparable to an industrial standard n^+pp^+ process. It starts by a texture (isotexture or random pyramids) etch of the surface. Then the front-surface field is formed by phosphorus diffusion in an infrared conveyor belt furnace from a spin-on source, resulting in 55-70 Ohm/sq. front surface field. Subsequently, rear side polishing etch, is carried out followed by the phosphorus glass removal and the PECVD SiN_x anti-reflection coating deposition on the front side. This process sequence does not further require wafer dicing or other methods for junction isolation, and thus the entire initial wafer area is used. The silver grid was then screen-printed on SiN_x front side, followed by screen-printing of Al on the whole rear side of the cell. Both contacts were co-fired in an infrared conveyor belt furnace, thus forming also the p^+ junction at the rear. The Process flow chart is and a schematic cross section of our Al back junction solar cell is shown in Figure 1.

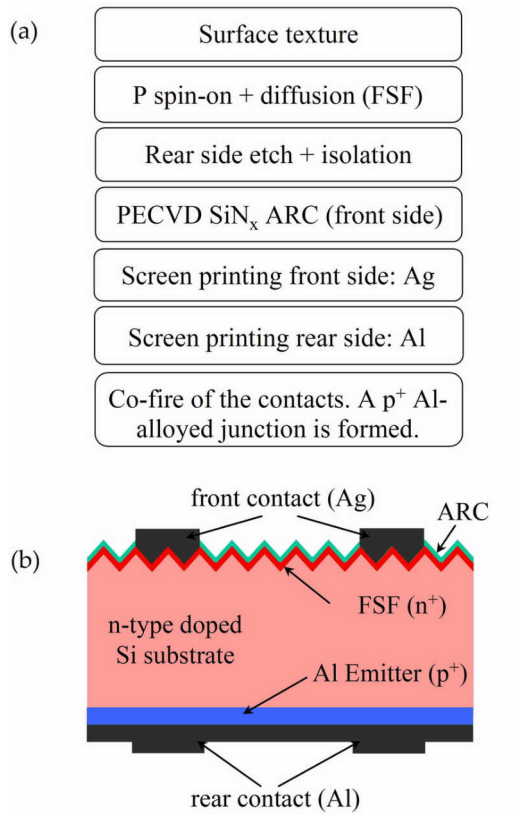

Figure 1: Process flow chart (a) and the schematic cross-section (b) of our standard back junction cell.

3 CELL RESULTS

Table I summarizes the solar cell parameters of the best results obtained for mc-Si and FZ substrates. It is observed that the highest efficiency is obtained for high substrate resistivity. This is in agreement with model calculations [4,8], which show that, in order to benefit from the full potential of this type of solar cells, the wafer resistivity should be higher than 10 Ωcm (with a thickness of less than 200 μm). The thicknesses of the solar cells presented in Table I are typically between 165-185 microns. On the other hand it is important to know what limits the efficiency at lower substrate resistivity, especially for multicrystalline substrates. To understand this, we first investigated the internal quantum efficiency (IQE) of the cells shown in the upper part of Table I (above the dashed line). These cells have been fabricated in the same run and have received our industrial standard phosphorous FSF diffusion of 55-63 Ohm/square. Figure 2 shows the experimental IQE (symbols) together with the PC1D fit (lines) using a measured front doping profile and surface reflection (shown typically in Figure 3), and assuming a constant Al doping profile for the rear junction. The relevant fit parameters for the modelling are the bulk lifetime and the front surface recombination velocity (SRV). Since for monocrystalline wafers the bulk lifetime is very high (>1 ms), it does not limit the IQE at lower wavelengths regime, where it is remaining completely determined by the SRV. The fit to experimental data reveals a SRV of $6.0(\pm1)\times10^5$ cm/s for both FZ wafers with resistivity of 3.8 and 30 Ohm-cm, respectively. Hence, the difference

Table I: Parameters of the best fabricated solar cells on FZ and mc-Si n-type substrates. The area of the solar cells amounts to 156.25 cm^2 for mc-Si cell and 148.5 cm^2 for FZ cells.

Si	ST	ρ [Ωcm]	Jsc [mA/cm²]	Voc [mV]	FF [%]	η [%]
mc	IS	0.8	19.77	589	73.7	8.6
mc	IS	12	29.7	580	72.1	12.4
FZ	IS	3.8	30.74	620	77.9	14.9
FZ	IS	30	34.18	621	77.4	16.4
FZ	IS	31	33.27	633	78.8	16.6*
FZ**	RP	31	35.53	632	77.4	17.4*

ρ - base resistivity; ST – surface texture; IS – isotexture etch; RP – random pyramids texture etch.
*Values independently confirmed at Fraunhofer ISE CalLab, Freiburg, Germany. **This cell has an area of 140 cm^2 after dicing away the unprinted Al area on the rear side.

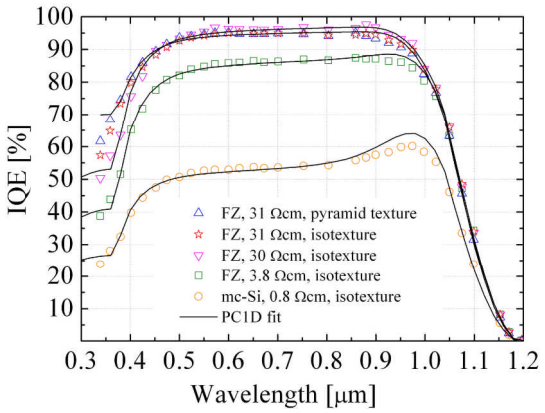

Figure 2: Internal quantum efficiency (IQE) data of the solar cells from Table I (symbols) and its PC1D fit (lines), taking into account the measured front doping profile, surface reflection, wafer resistivity, and wafer thickness.

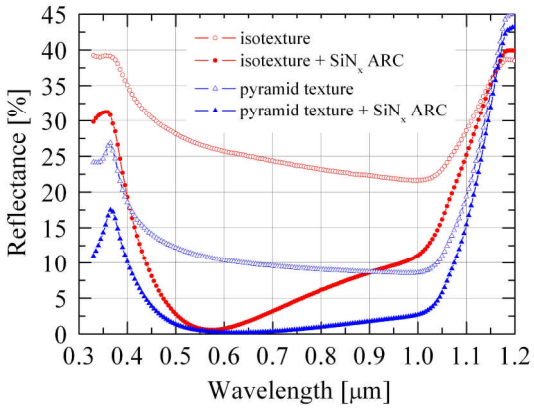

Figure 3: Measured front surface reflectance of an isotexture and random pyramids etched surfaces with and without SiN_x antireflection coating layer on top (see legend).

observed in IQE or in power conversion efficiency between these wafers is accounted only by the difference in their substrate resistivity. Such a good agreement

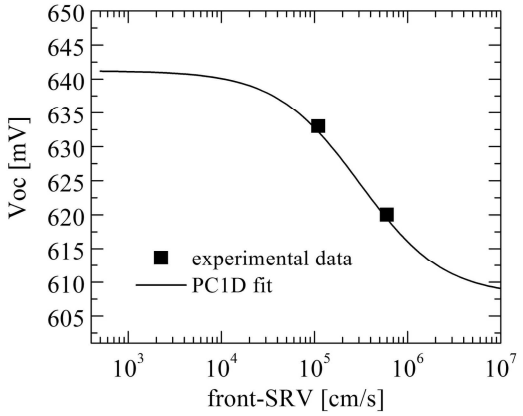

Figure 4: Calculated Voc as a function of surface recombination velocity for an n-type FZ with a resistivity of 30 Ωcm. The parameters used in the calculation are those found by fitting the experimental data of Figure 2.

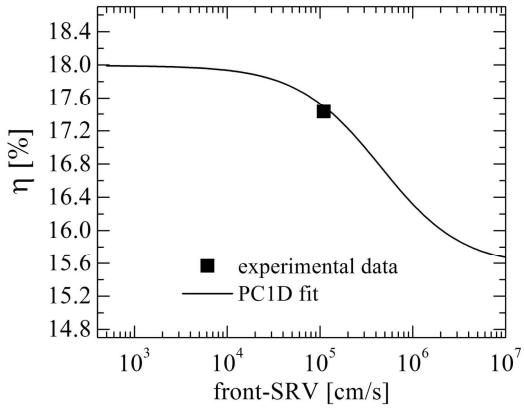

Figure 5: Calculated solar cell efficiency as a function of surface recombination velocity for an n-type FZ with a resistivity of 30 Ωcm. The calculation is done considering a FF of 78.8% and a random pyramid texture etch surface. The parameters used in the calculation are those found by fitting the experimental data of Figure 2.

between calculated and experimental data allows identifying SRV as the limiting parameter for solar cells efficiency based on monocrystalline substrates and having similar Al rear junction.

The bulk lifetime must be taken into account, however, when we analyze the current-voltage or IQE data of the solar cells fabricated on multicrystalline wafers. The IQE fit of multicrystalline cell from Table I reveals the same SRV value as that obtained for monocrystalline cells above (6.0×10^5 cm/s), but with a considerable lower bulk lifetime of only 28 μs (as obtained from PC1D fit). It has been shown that the ratio of diffusion length and substrate thickness (L_d/d) must be higher than 2.5 to ensure that the cell performance is not limited by the wafer quality [11]. Thus, to meet these conditions, the effective lifetime of the multicrystalline substrates must be higher than 130 μs. Hence, besides resistivity, the bulk lifetime is another important factor that limits the efficiency of n-type multicrystalline silicon solar cells with a rear side emitter.

Currently we are investigating ways to reduce SRV of these types of cells and, thus, to further improve their efficiency. In the lower part of Table I (below dashed line) the best results of this effort are shown for cells fabricated on FZ wafers. It is observed that approximately 12 mV higher Voc and up to 1.4% higher FF are achieved by engineering our phosphorous FSF diffusion and improving our cell process. As a result of this new process, the SRV was further reduced to $1.0(\pm1.0)\times10^5$ cm/s (by fitting the IQE data). Furthermore, in order to explore the full potential of our improved cell process we have fabricated solar cells having a random pyramids texture etch surface. The conversion efficiency reached in this case is 17.4%, independently confirmed at Fraunhofer ISE CalLab, Freiburg, Germany. To our knowledge, this is the highest efficiency obtained for n-type silicon solar cells featuring a screen-printed aluminium rear-emitter and it even outperforms the results obtained on p-type (n^+pp^+) monocrystalline substrates fabricated in a similar way in our lab (data not shown).

Figure 4 shows the model calculations for Voc as a function of SRV. The SRV has been determined from the PC1D fit of the IQE data (as shown in Figure 2). As demonstrated by the model calculation the gain in Voc of the cell is indeed due to a lower SRV as a result of our improved phosphorous FSF diffusion. Moreover, the Voc of 633 mV is among the highest measured on large area (148.5 cm^2) solar cells featuring a screen printed contacts and is already close to the Voc limit (about 642 mV) of an Al-alloyed rear full area emitter cell [10, 12]. Additionally, in Figure 5 the model calculation for the conversion efficiency versus SRV is shown. The starting point of this calculation was the experimental data of the 17.4% efficiency cell (see Table I). It is clear from the figure that efficiencies of approximately 18% can be obtained even after fully minimizing SRV. With the FF reaching 79% there are two major factors left that limit the efficiency of this state-of-the-art industrial screen-printed aluminium rear-emitter cell to only 18%: First is the limitation imposed to Jsc due to metallization shading of the front surface (which amounts to 8.0% in our cells), and second is the fundamental limitation imposed to Voc (and Jsc), of only approximately 642 mV, due to recombination that occurs in the Al-alloyed emitter. Cuevas et al. have reported that the recombination current density in the p^+ region formed by screen printed aluminium and alloying can not be lower than approximately 500 fA/cm^2. Such recombination can drastically limit the Jsc and Voc of a cell even if SRV is minimized and high quality wafers are used [10, 12].

Work is underway to further improve the efficiency of these cells towards 18%, as indicated by model calculation shown in Figure 5. We also further investigate multicrystalline substrates using this process to reveal how lifetime and wafer resistivity limit the obtaining of a good solar cell performance for multicrystalline wafers. It is expected that 130 μs lifetime, which has been measured already, is good enough to reach high efficiencies on multicrystalline substrates.

4 CONCLUSION

We have demonstrated that a low cost process of

fabricating n-type solar cells based on the Aluminum rear-emitter concept leads to a new record efficiency of 17.4% for large area (140 cm^2) monocrystalline FZ substrates. Moreover, by improving the front surface passivation higher efficiencies could still be realized, as demonstrated by our model calculations. High efficiencies may also be conceivable on n-type multicrystalline substrates after material optimizations, such as higher resistivity and increased lifetime (and improved homogeneity).

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